RCA ENGINEER

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APRIL—MAY, 1962

OBJECTIVES

To disseminate to RCA engineers technical information of professional value.

●

To publish in an appropriate manner important technical developments at RCA, and the role of the engineer.

●

To serve as a medium of interchange of technical information between various engineering groups at RCA.

●

To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions.

●

To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field.

●

To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management.

●

To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

OUR COVER

Dr. H. S. Veloric, Mgr., Silicon Computer Products, Semiconductor and Materials Division, Somerville, N. J., and a grouping of advanced devices and microelectronic circuit packages. First row (left, front to rear): Ge, Si, and GaAs transistors. Second row: a transistor wafer, a high-power transistor, a GaAs power rectifier, and a minimodule (transistor on top, conventional components potted inside, to form circuit). Third row: another transistor wafer, a GaAs rectifier, a micromodule (wafer components stacked and potted inside to form circuit), and another transistor. Fourth row: HF low-inductance power transistor, a GaAs solar cell, magnetic memory cores imbedded in aluminum and plastic channel (equivalent to a 12-bit word), and a custom-made miniature-circuit package (potted conventional components). Last row, starting at right front: two ceramic integrated-circuit wafers, a Hall bridge, and (at pencil-point) three tunnel-diode integrated circuits.

Interdivisional Cooperation

To further understanding of a commercial organization, it is often helpful to draw parallels with the inorganic world. I have found this to be especially true in addressing the theme of interdivisional cooperation presented here.

If, for a moment, we consider our Princeton Laboratories and our component and equipment divisions as the emitter, base, and collector regions of a gigantic semiconductor device designed to amplify ideas into components, and components into equipment, we can proceed at once to study their interrelation in terms of the interfaces at which they meet.

As is true of the junctions of a transistor, these divisional interfaces can be irregular, at times, and the cause of frequent breakdowns; or they can be uniform, high-current contacts and the sources of continued progress for us all—*both* as individual divisions and as a corporate enterprise.

Supporting this viewpoint are many examples of interdivisional cooperation, of which the tunnel diode is perhaps the most remarkable. Here is a device that in four short years has gone from a laboratory sample at Princeton to a major product whose potential benefits are under investigation throughout RCA. Electronic Data Processing is developing tunnel-diode memory and logic circuitry for a computer that will be 100 times faster than any now in existence. Defense Electronic Products is considering using tunnel diodes to build a high-speed computer with very low power dissipation for earth satellites. The Electron Tube Division already features these diodes in a new line of microwave amplifiers and oscillators. The Home Instrument Division has considered them for use in TV tuners.

Everywhere, new products, new profits, and new prestige have resulted for us from this new device. Its actual development, manufacture, and use, however, have depended jointly on the scientific thrust of our Princeton research staff, the technological and production skills of the Semiconductor Division, and the creative applications engineering of the many RCA equipment divisions.

I should like to make a special plea that this kind of cooperation *be further encouraged* not only to include areas where we have an obvious coincidence of interest, but to include as well those areas where our mutual interest is perhaps less clear—*but no less real*. May I suggest that whether the subject is a new product line, an improved manufacturing process, or the exploitation of a new scientific principle, we can make more effective use of our resources—individually and collectively—if we recognize more clearly that the divisional interfaces which separate also join and *may greatly benefit* our many diverse activities.

For its recognition of this fact and for the role it plays in making us all aware of the importance of *interdivisional cooperation*, I commend the staff of and the contributors to the RCA ENGINEER.

Dr. Alan M. Glover
Vice-President & General Manager
Semiconductor & Materials Division
Radio Corporation of America

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RCA ENGINEER

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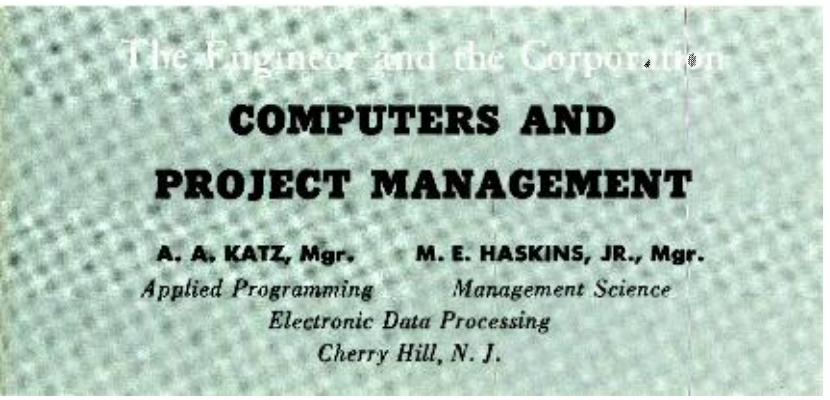
APRIL - MAY 1962

A TECHNICAL JOURNAL PUBLISHED BY **RADIO CORPORATION OF AMERICA,** PRODUCT ENGINEERING 2-8, CAMDEN, N. J.

THE EVER-INCREASING technological complexity of modern business is creating several trends that are of great significance to engineers and managers: One is the application of scientific techniques and the "engineering approach" to management problems—including the increasing professional role of engineers and scientists in management. Another is the trend in management emphasis from the *task* to the *function* to the *project*—resulting, in large part, from the usefulness of computers in integrating the ever-increasing complexity of relationships.

This latter trend has placed a premium on good management: the *task* emphasizes individual jobs, such as wiring a panel; the *function* focuses on an activity, such as accounting or sales; but the *project* considerably broadens the scope of management control, since it cuts across and integrates functions according to specific major goals to be reached. It is top management on a small scale. Thus, this trend is creating great pressure for more-scientific



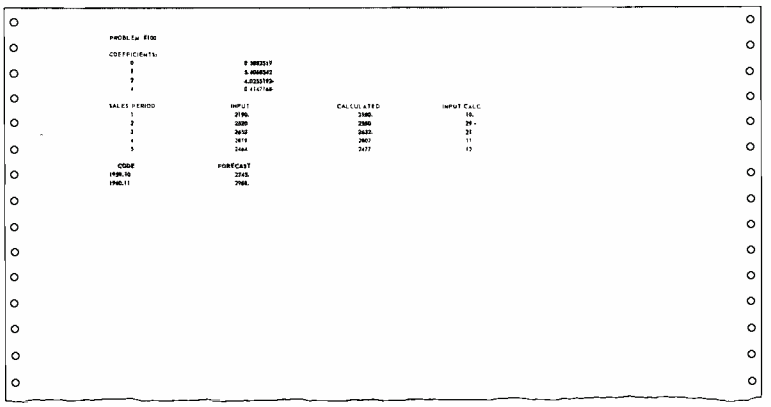
project-management techniques and more direct application of computers to the management job.

The management job of the project manager is twofold: 1) *to lead* by interpreting policy, motivating behaviour, and initiating action; and 2) *to administer* by determining and balancing goals and resources.

The first activity is a human side of management requiring judgment and integrity—without which no manager can succeed. The second activity is no less important, *but is subject to application of scientific principles.* It can be viewed as a process of making decisions (planning, directing, controlling) and getting the most profitable and efficient use of the available resources (men, money, materials, machines, time, ideas).

There is nothing startling in the above statement of the project manager's problems, although their order of importance changes from project to project and from time to time. There is, however, quite a bit new about the *solutions* to these problems—new approaches, new techniques, and new applications for computers. It is our intention to show herein how the above trends in management are manifesting themselves through what has been called *management science*—particularly as related to the use of computers as a tool of management.

Fig. 1—A computer output from the SALES FORECASTING package.



THE MANAGEMENT-SCIENCE APPROACH—BEFORE COMPUTERS

There have been a good number of excellent management tools developed that do not require computers for their successful implementation. A few come readily to mind.

For decision-making, scientific management tools for planning, directing, and controlling have been developed as long ago as 50 BC (before computers). Names like Taylor, Gilbraith, and Gantt are still fairly well known.

In planning, Gantt Charts have been in wide use for many years. They represent the start- and end-dates of a complex of activities and show the relative spread of jobs, thus indicating the needs for various resources. Break-even analyses utilizing graphs have been successfully used to plan the profitability of operations and to portray basic price-volume relationships.

In directing, traditional accounting systems and budgets have served management well. Although reports have progressed from giving complete data on all items reported to reporting by exception, accounting reports suffer mostly for providing information "after-the-fact." Also, reports have traditionally been prepared on a cyclical basis (each week, month, quarter, etc.).

In control, some of the principles of statistical quality control have been applied to inventory and production problems. More recently, the *Line-of-Balance* method' is providing an excellent vehicle for planning and especially for controlling the progress of projects.

For resource-allocation, time clocks were an early pre-computer application of manpower control, budgets reflect the spectrum of dollar resources, formulas for calculating optimum economic order quantities are widely used, preventive maintenance concepts have been useful in making important purchasing decisions, and bar graphs or Gantt charts have been popular for showing time relationships.

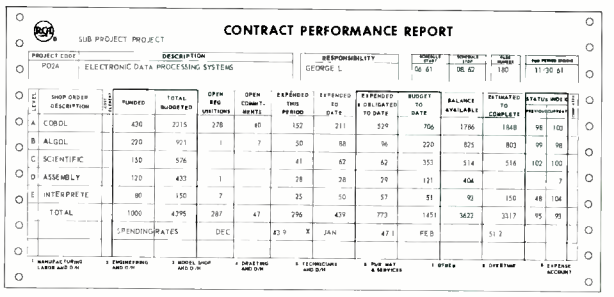
MANAGEMENT SCIENCE—SINCE COMPUTERS

The entrance of computers into the realm of management science in no way cancels the past—rather it is merely the introduction of a new tool which allows present horizons to be expanded. For decision-making, computers have spurred several breakthroughs and made possible and practical the application of a number of well-known mathematical techniques. These techniques, applied to management, cover the areas of planning, directing, and controlling.

Planning and Scheduling

Now it is possible to plan on sound forecasts made by a mathematical model of the market for each product line. The model is built by using a computer SALES FORECASTING package that will select from as many as forty economic or demographic indices supplied by marketing management. The process is one of trial and error involving the power of mathematics, the speed of the computer, and the judgement and insight of management. Fig. 1 shows a typical computer output that indicates which indices were selected, the weight assigned to each, their accuracy in predicting past history, and a forecast of several future periods.

Having determined forecasts by products and by regions, it is now possible to use the computer to select the optimum



CONTRACT PERFORMANCE REPORT

SUB PROJECT PROJECT

PROJECT CODE	DESCRIPTION	RESPONSIBILITY	BUDGET START	BUDGET END	PLAN NUMBER	PLAN PERIOD ENDING
P02A	ELECTRONIC DATA PROCESSING SYSTEMS	GEORGE L.	06 61	08 62	180	11-30-61

LEVEL	SHOP ORDER DESCRIPTION	ACCT. NUMBER	FUNDED	TOTAL BUDGETED	OPEN REQ. UNITIONS	OPEN COMMIT-MENTS	EXPENDED THIS PERIOD	EXPENDED TO DATE	EXPENDED & OBLIGATED TO DATE	BUDGET TO DATE	BALANCE AVAILABLE	ESTIMATED TO COMPLETE	STATUS INDEX (PERFORMANCE)	STATUS INDEX (EXPENDITURE)
A	COBOL		436	2015	278	81	152	211	529	706	1786	1848	98	103
B	ALGOL		220	921	1	7	50	88	96	220	825	803	99	98
C	SCIENTIFIC		150	578			41	62	62	353	514	516	102	100
D	ASSEMBLY		120	433	1		28	28	29	121	404			7
E	INTERPRETE		80	150	7		35	50	57	51	92	150	48	104
	TOTAL		1000	4395	287	47	296	439	773	1451	3622	3317	95	95
	SPENDING RATES		DEC			43 9	X	JAN	47 1	FEB		51 2		

1 MANUFACTURING LABOR AND O/H 2 ENGINEERING AND O/H 3 MODEL SHOP AND O/H 4 DRAFTING AND O/H 5 TECHNICIANS AND O/H 6 PUR MAT & SERVICES 7 OTHER 8 OVERTIME 9 EXPENSE ACCOUNT

Fig. 2—A computer output from APEX (Analysis of Performance and EXpenditure).

allocation of product by warehouse or production at each factory by linear programming.

At that point, plans can be translated into projects, each with a general blueprint. This blueprint can eventually be assigned calendar dates and converted into charts for Line-of-Balance control. First, however, the blueprints are converted into programs and schedules by representing them as a network[2] of interrelated activities and then using a PERT/RESOURCES computer package to calculate whether deadline dates can be met, at what cost, and what resources will be required.

When several feasible programs for each product are obtained (it's easy and economical to plan alternative actions when a computer is used), they can be tested out on a model of the business. The so-called business model is also the result of another computer package — PROTOTYPE BUILDER — which makes it relatively simple for a knowledgeable executive to translate his own mental picture of how the business functions into a mathematical computer model, simply by using various pre-packaged blocks according to the conditions of his business. Once the model is built and tested to see that it reacts to stimuli just as the real-life business, it becomes a powerful tool for strategic decision-making and for testing out alternative project programs.

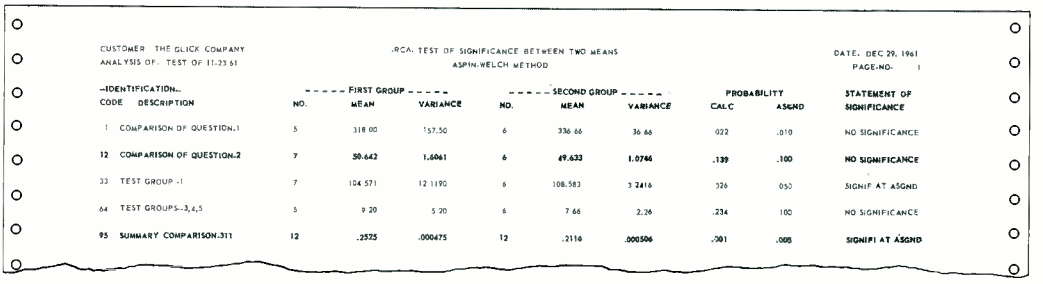
Thus, using computers, management scientists have evolved a discipline of planning and scheduling. It separates the planning from the scheduling — the former being done mostly by humans, the latter by the computer. Relationships between jobs or activities are made clear by network charting (PERT). Doubts in estimating are handled statistically by submitting optimistic, realistic, *and* pessimistic estimates, which the computer converts into probabilities (Fig. 4). The computers also make it practical to consider and evaluate various alternate plans.

Directing: Reporting and Decision-Making

Directing operations has also been materially improved by the triple power of applied mathematics, computer packages, and human know-how. First of all, because plans and programs can almost be entirely "electronicized," changing or revising them becomes a simple task — even for the most complex plans. Then, too, there seems to be a trend for noncyclical reporting (i.e. reporting on multiples of scheduled dates such as at the quarter, half, and three-quarter points) in addition to feed-forward type of information that shows where trouble is most likely to crop up *before the fact*. And, there is the relatively new concept of *responsibility reporting*.

Responsibility reporting gives each manager the detailed information he needs to control the work for which he is responsible. Exactly the same set of data is used as that which will be condensed to produce reports for the next higher level of management. A computer package — APEX — does this for seven levels of management, while keeping track of individual managers' names so that each report is headed by the name of the manager responsible for the performance (Fig. 2). The computer package also permits individual elements of cost (such as drafting or travel expense) to be accumulated vertically through several levels of management.

One of the most difficult tasks in directing large projects is that of making sequential decisions. When things seem to be going well, there is a human tendency to not depart from the norm of previous decisions, often with the result that things get in a pretty bad state when trouble is finally recognized. Conversely, when the situation has been bad, the human tendency is to keep changing the nature of decisions at the slightest deviation, even though — in actuality — the previous sequence of decisions does not (statistically) warrant such concern. A computer package called GIST allows for testing changes in a number of critical factors, at the manager's option. The package will



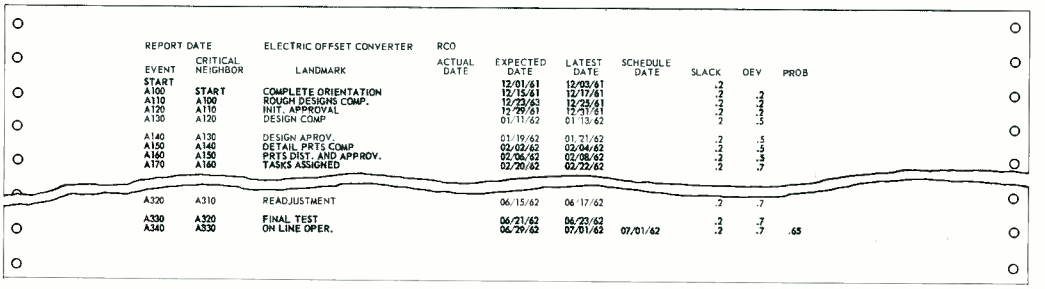
CUSTOMER THE GLICK COMPANY
ANALYSIS OF: TEST OF 11-23 61

RCA: TEST OF SIGNIFICANCE BETWEEN TWO MEANS
ASPIN-WELCH METHOD

DATE: DEC 29, 1961
PAGE-NO- 1

IDENTIFICATION CODE	DESCRIPTION	FIRST GROUP NO.	FIRST GROUP MEAN	FIRST GROUP VARIANCE	SECOND GROUP NO.	SECOND GROUP MEAN	SECOND GROUP VARIANCE	PROBABILITY CALC	PROBABILITY ASGND	STATEMENT OF SIGNIFICANCE
1	COMPARISON OF QUESTION-1	5	318 00	157.50	6	336 66	36 66	022	.010	NO SIGNIFICANCE
12	COMPARISON OF QUESTION-2	7	50.642	1.6061	6	49.633	1.0746	.139	.100	NO SIGNIFICANCE
33	TEST GROUP -1	7	104 571	12 1190	6	108.583	3 2416	526	050	SIGNIF AT ASGND
64	TEST GROUPS-3,4,5	5	9 20	5 20	6	7 66	2.26	.234	100	NO SIGNIFICANCE
95	SUMMARY COMPARISON-311	12	.2525	.000475	12	.2116	.000506	.001	.005	SIGNIFI AT ASGND

Fig. 3—A computer output from GIST.



REPORT DATE ELECTRIC OFFSET CONVERTER RCO

EVENT	CRITICAL NEIGHBOR	LANDMARK	ACTUAL DATE	EXPECTED DATE	LATEST DATE	SCHEDULE DATE	SLACK	OEV	PROB
START				12/01/61	12/03/61		.2		
A100	START	COMPLETE ORIENTATION		12/15/61	12/17/61		.2	.2	
A110	A100	ROUGH DESIGNS COMP.		12/23/61	12/25/61		.2	.2	
A120	A110	INIT. APPROVAL		12/29/61	12/31/61		.2	.2	
A130	A120	DESIGN COMP		01/11/62	01/13/62		.2	.5	
A140	A130	DESIGN APROV.		01/19/62	01/21/62		.2	.5	
A150	A140	DETAIL PRTS COMP		02/02/62	02/04/62		.2	.5	
A160	A150	PRTS DIST. AND APPROV.		02/06/62	02/08/62		.2	.5	
A170	A160	TASKS ASSIGNED		02/20/62	02/22/62		.2	.7	
A320	A310	READJUSTMENT		06/15/62	06/17/62		.2	.7	
A330	A320	FINAL TEST		06/21/62	06/23/62		.2	.7	
A340	A330	ON LINE OPER.		06/29/62	07/01/62	07/01/62	.2	.7	.65

Fig. 4 — Beginning and end of a computer output from PERT.

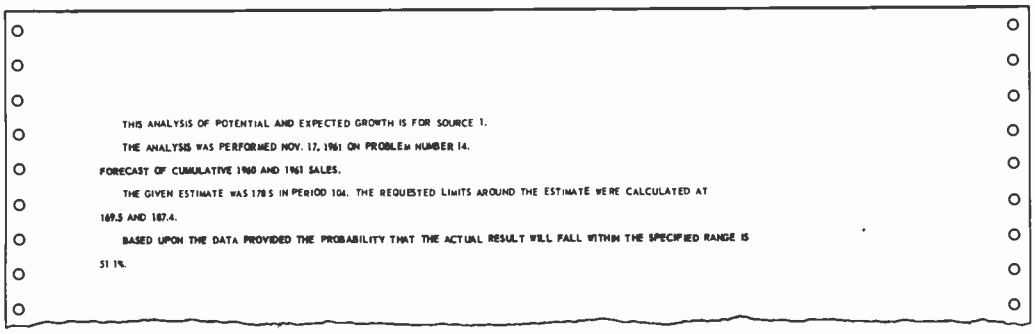


Fig. 5—A computer output from PEG (Potential and Estimated Growth).

indicate whether, statistically, there has been any significant difference between sequential decisions (Fig. 3). This tool will not help humans to make a decision, but it does provide an objective way of *appraising the results* of decisions.

Controlling

The art and science of controlling has been significantly improved by the advent of computers. First, the computers have allowed for more integration between the planning and controlling of projects. Second, reports can be prepared much faster than before, so that even after-the-fact information can still be current and useful. Third, computers have made it practical to keep closer control on the pace or rate of flow of the business — for example, sales.

Perhaps the best-known breakthrough in management control resulting from the utilization of computers is PERT — the *P*rogram *E*valuation and *R*eview *T*echnique. It is both a planning and a control tool, thus making coordination between the two activities almost automatic. As mentioned previously, the PERT computer package calculates the probabilities for meeting deadlines. The output (Fig. 4) also indicates the *expected date* for the completion of each activity or event, the *latest date* on which each *should* be completed in order to meet deadlines, and even more important, the *slack* associated with each.

The slack shows the amount of time by which an activity or event can be delayed and still not imperil scheduled dates. If the slack is zero, the associated activity or event cannot be delayed without expecting an equivalent delay in the completion date. A negative slack indicates that the project is running behind and that the deadline will not be met unless time is made up. The control features of this technique are that it indicates those activities or events (usually a small minority) which are critical and must be watched and, likewise, those that show slack and the resources for which may be traded-off to bring negative slack activities or events back in line.

It is doubtful if anyone reading this could not point out several examples of reports being prepared by computers in a much shorter time than they had been prepared manually. It is not merely the tremendous speed of the computer that makes this possible; it is also the psychological (or perhaps mechanical) factor that the computer run cannot be made until *all* the input has been received, which forces those who submit input information to be punctual.

Because of their speed and accuracy, computers can be used not only to record data and process it into useful control information, but also to check the data itself to see that it is adhering to the planned rate-of-flow of the business. If historical data is available, rather precise statistical controls can be established. Even when past history is not available, it is possible to check actual results versus forecasts on a short-cycle basis, such as weekly. For example, Fig. 5 shows output from PEG, a computer package that evaluates a forecast on the basis of available data *plus* human intuition or subjective information. Its output shows the probability that can be ascribed to any forecast on the basis of both these inputs.

Allocation of Resources

The allocation of resources has always been a difficult task for managers. It has been difficult principally for two reasons: 1) the human mind can only retain and handle limited amounts of information or complexity (using paper and pencil, charts, and other visual aids helps, but they also have their limit) and 2) the amount of work required to do a good job requires considerable time and/or staff if done "by hand" (as a result, "real good jobs" are the exception rather than the rule).

Computers also have limits as regards the size or complexity of the job they can do — although this limit greatly exceeds that of humans. Actually, the biggest limiting factor on computers today is *the knowledge that management has* about how the business *really* works, the interrelation-

ARTHUR A. KATZ obtained his education at Colby College where he received his BA in 1946. He has studied electrical engineering at New York University and advanced mathematics at the University of Pennsylvania. Mr. Katz is experienced in the utilization of electronic data processing equipment, staff organization, administration, and system analysis. He has practical experience as manager of technical groups of analysts, operations researchers, scientists and programmers. He has planned, budgeted, organized, staffed and directed EDP centers, and has consulted nationally in the analysis of EDP requirements. Mr. Katz is a member of the Association for Computing Machinery and was a Council Member in the year 1957. He is a member of the Institute for Management Sciences, and is currently Manager of Applied Programming for RCA Electronic Data Processing.

M. E. HASKINS, JR. graduated from the Polytechnic Institute of Brooklyn in 1949 with a BSEE. He joined the Westinghouse Corporation and, after completing its Graduate Student Course, started his work career as a Sales Engineer. He later transferred to the Westinghouse Lamp Division Headquarters where he worked in Commercial Engineering. After receiving his MBA from the New York University Graduate School of Business Administration, he worked on production and inventory-management and operations-research problems. Joining the Computer Applications Research Department of Philco Corporation, he gathered experience in the application of computers in the areas of purchasing, production scheduling, material control, and management controls. He joined RCA in 1959 as a Senior Methods Specialist in the Applied Science section (which was responsible for OPERATION BALLOT). In late 1960 Mr. Haskins was named manager of the Management Science group, which is engaged in designing and implementing computer programs as tools of management.

A. A. Katz

M. E. Hoskins

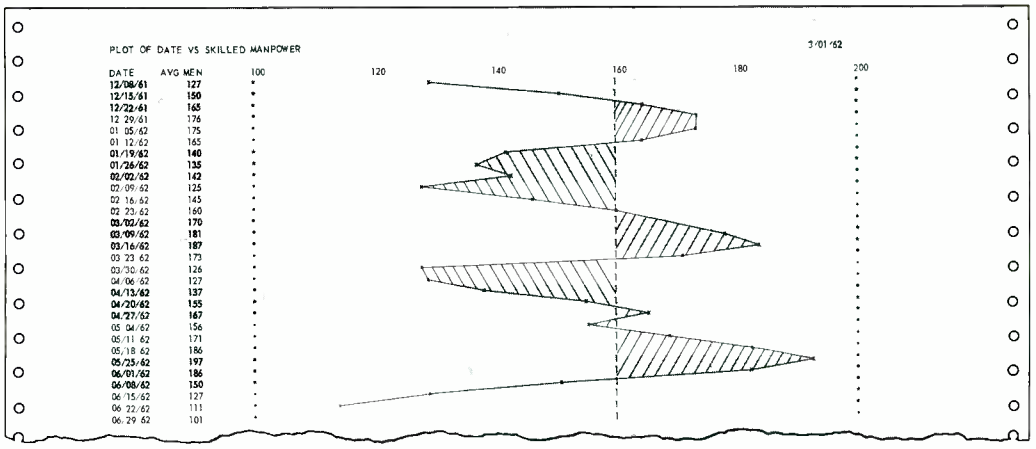


Fig. 6—An output from PERT/RESOURCES. Computer prints out the data, as well as data points for the graph that the user can then fill in.

ships between activities, what cause is responsible for what effect, etc.

Because of this, most practical computer packages do not attempt to do the entire job, but rather handle those mental manipulations too complex for humans to handle in any practical time limit. Thus, a computer program such as PERT/RESOURCES will plot output such as shown in Fig. 6 on a number of resources associated with a complex of activities. It would be relatively easy, where only a few variables are involved, for a manager to calculate the time relationships involved and even the probabilities; however, in a more complex situation, perhaps with many types of machines or classes of labor incorporated simultaneously, this job would be laborious indeed, for a manager, if not impossible. Yet, this is exactly what project managers must do — one way or another. By looking at computer outputs for each resource (Fig. 6) management can use its energies to think up *ways and means for improving* the situation rather than spending time just finding out what the situation is.

In some areas of business, as in personnel work, the amount of information (about hundreds or even thousands of individuals) can be so large relative to the human capabilities of the office staff, that management often cannot do as good a job as it "knows how." Yet, one of the most vital problems in directing companies today is the full utilization of human resources. As Peter Drucker has pointed out: "In more and more cases, the supply of qualified people, rather than the supply of money, materials or markets, is becoming the major limit to the ability of business to realize its goals."[3] Thus, we find numerous cases where new employees (who know nothing about company operating policies and facilities) are hired because they have some specialized knowledge — yet there are individuals presently on the payroll *with* that specialized knowledge (*and* who *are* familiar with how the company operates and know whom to see within the company to get material assistance). Unfortunately, this fact is not known nor is there time to spend looking through reams of records — it is easier to hire a new person.

This example can probably be repeated in other areas of business besides personnel. Wherever it exists is a fertile area for the use of computers. For example, in the personnel area, there is a computer package known as the HUMAN RESOURCES ANALYZER that will digest all the data available on an organization's personnel. Then, as needs for different kinds of human-resources information arise, the computer analyzes the stored data and prints out the needed information — in its original context (Fig. 7).

SUMMARY

It is difficult to separate cause and effect in the rapid strides that are being made in management science. It is a truism that fantastic results can come only from fantastic problems. While not wishing to detract from the excellent work already done by management scientists, it must be admitted that these computer aids to better management must be put into effect *and made to work* by operating managers before they can be improved upon through even better methods that might then be developed by the management scientists. Thus, as in walking, it takes two legs, each taking one step at a time, to get places.

Computers hold a tremendous potential for management — *after* management realizes that their real objective is to accept computers as another tool for the management job, *not to delegate part of their job to it.* It remains then for the computer to be applied with this thought in mind: it must be adapted to the application, *not* the application to the computer — the real purpose of modern management science.

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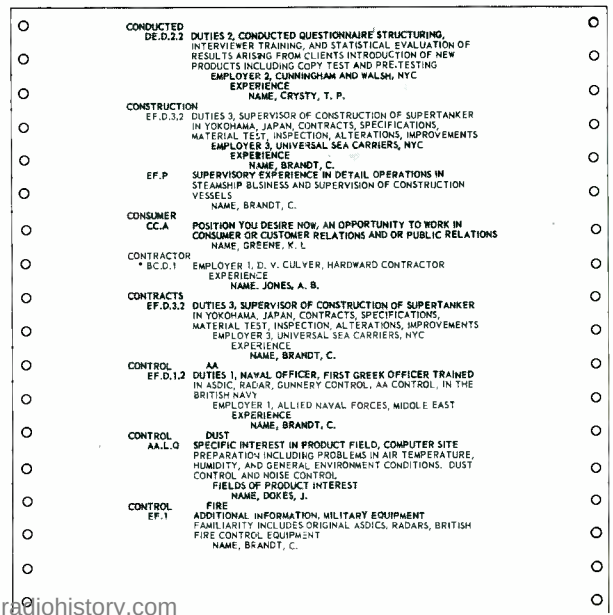
3. "Integration of People and Planning," *Harvard Business Review*, Nov.-Dec. 1955.

Fig. 7—Portion of a computer output from the HUMAN RESOURCES ANALYZER package.



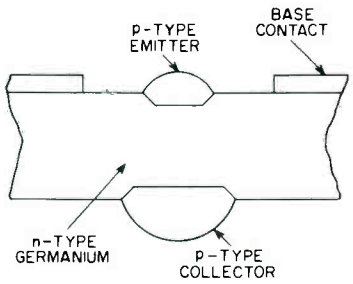


Fig. 1—Cross-section of a p-n-p alloy junction transistor.

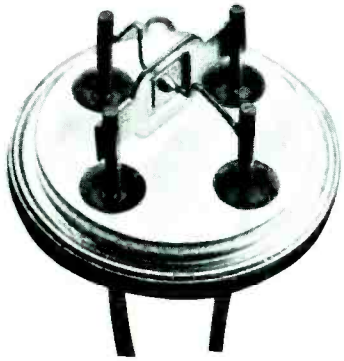


Fig. 2—Germanium alloy transistor structure.

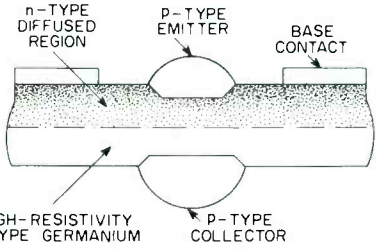


Fig. 3 — Cross-section of alloy drift-field transistor.

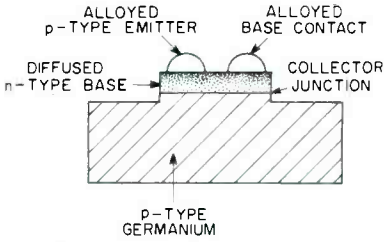


Fig. 4 — Cross-section of dot alloy mesa.

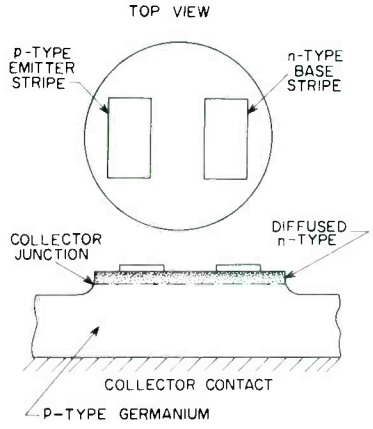


Fig. 5 — Cross-section of p-n-p germanium evaporated-stripe mesa.

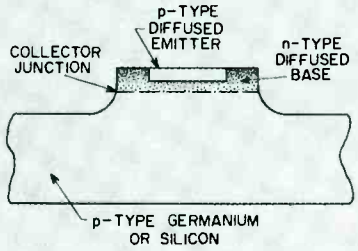


Fig. 6 — Cross-section of p-n-p germonium or silicon double-diffused meso transistor.

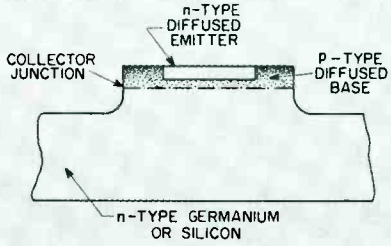


Fig. 7 — Cross-section of n-p-n germanium or silicon double-diffused mesa transistor.

THE CONTINUING REVOLUTION IN SEMICONDUCTORS

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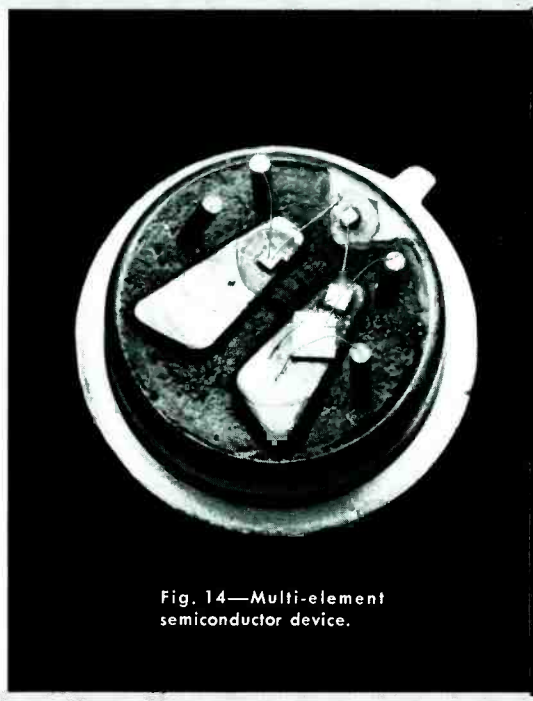

Fig. 14—Multi-element semiconductor device.

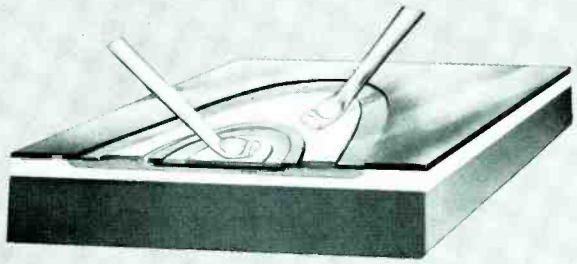

Fig. 8—Planar-type n-p-n silicon transistor with epitaxial layer.

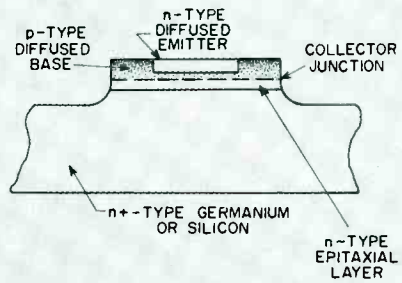

Fig. 9 — Cross-section of n-p-n transistor with epitaxial layer.

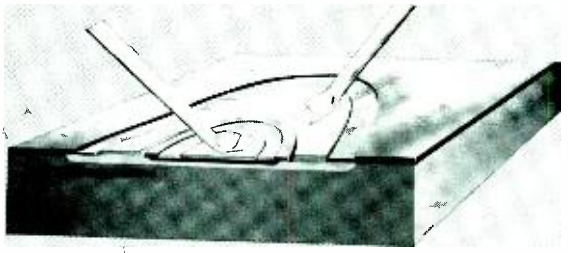

Fig. 10 — Planar-type n-p-n silicon transistor with diffused collector.

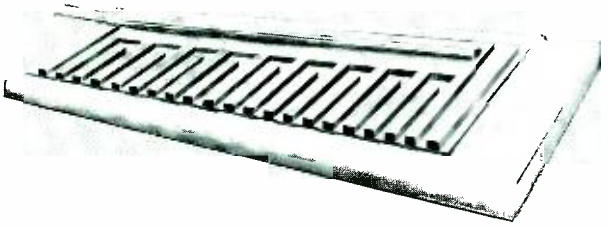

Fig. 11 — Planar-type triple-diffused n-p-n silicon transistor with interdigitated emitter and collector.

Several times in the past few years the revolution in semiconductors seemed to slow down. Each time, however, a new development arose to keep the pot boiling. A continuation of this rapid pace now and in the near future appears certain. This article reviews the present state of the semiconductor art and attempts to look forward to the immediate and the distant future.

ALTHOUGH the pace of technological change in semiconductors has been rapid, some of the earliest devices have held on tenaciously. Typical is the technically obsolete point-contact transistor presently doing an excellent job in certain equipments. The cost of re-engineering such equipments to accommodate newer types cannot be justified. Of course, the point-contact transistor is not being used in modern designs.

The same pattern of long application life is true, to a greater degree, for the grown-junction transistor. Following the point-contact method, the grown-junction technique was developed next for the manufacture of transistors. The early germanium grown-junction types used primarily in the consumer market have nearly disappeared today.

The first practical silicon transistor was the grown-junction type. The higher operating-temperature capabilities of the silicon types prompted designers to use them in many military equipments; as long as these equipments are produced, a continuing market will exist for the technically obsolete silicon grown-junction types. Certain characteristics of grown-junction types are difficult to reproduce in the modern mesa or planar structures, thus often preventing a direct substitution. The silicon grown-junction transistor is used sparingly for new designs.

Another situation exists in the historical third class of transistor structures—the alloy transistor (Fig. 1). Over the years, the germanium alloy transistor has reached a peak of refinement in its characteristics and reliability (Fig. 2). User prices have fallen to an extremely attractive level because of the very large volumes produced for the computer and consumer markets. For many years to come, the germanium alloy device will

DR. ROBERT B. JANES received his B.S. in physics from Kenyon College. He did graduate work in physics and mathematics at Harvard and at the University of Wisconsin, where he received a Ph.D. in 1935. He served as instructor in physics at Colgate University and as a research assistant at Wisconsin. Dr. Janes joined RCA at its Harrison plant in 1935. From 1935 to 1943, he was an engineer working on television camera tubes and phototubes. He was a member of the group that developed a phototube for the earliest proximity fuze. In 1943 he transferred to Lancaster where he was in charge of the group on television camera tubes. During this time the image orthicon and vidicon were successfully developed. In 1950, he became Manager of the Camera, Storage Tube, and Photo Tube group. From this group came many new image, multiplier, and storage tubes. In 1954, he was appointed Manager of Color Kinescope Development. From the intensive development program instituted in 1954 came the present color picture tubes. In 1956, Dr. Janes transferred to SC&M. Since then, he has held several engineering positions, and is presently Manager of Advanced Development Applications. Dr. Janes is a *Fellow* of the IRE and a member of Sigma Xi. In 1948, he received the *RCA Award of Merit*.

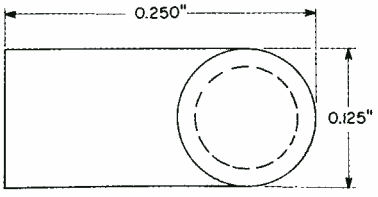

Fig. 12—Tunnel-diode package.

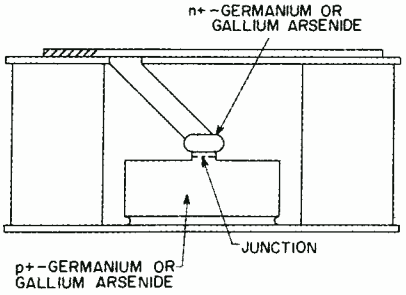

Fig. 13—Cross-section of tunnel diode.

be attractive to many areas: moderate-speed computers, the audio portion of consumer equipment, and a wide variety of industrial uses involving frequency ranges less than 1 Mc. In low- and medium-speed computers, the greater speeds of the more modern transistors can actually cause difficulty. Industrial applications of germanium alloy transistors will continue to grow at a slower rate, and prices will stabilize near their present levels.

The outlook for silicon alloy transistors is quite different. Except for a few specialized applications, there appears to be little future for silicon alloy transistors, since their characteristics are relatively poor; they are not expected to be used in volume applications.

LOW-POWER TRANSISTORS

In low-power transistors having a frequency response above that of germanium alloy types (greater than about 10 to 20 Mc) there have been many changes. The first attempt to provide a low-power, high-frequency device was the micro-alloy type; in this approach, the base width was closely controlled by automatic means to obtain a narrow base width W and, consequently, a high-frequency response. The micro-alloy type was the only high-frequency transistor available for a considerable period.

Alloy-Drift Types

Development of the alloy-drift transistor (Fig. 3) was next. This approach used a graded region in the base just below the emitter plus an intrinsic region near the collector. For use in an amplifier when low output capacitance and low base resistance are needed, the resultant characteristics were nearly ideal: high-resistivity base region near the collector, a low base resistance because of a low-resistivity base region at the emitter; and an improved high-frequency response caused by the graded base. The alloy-drift technique resulted in regular alloyed structures like the 2N247 and 2N384. Both types have found great usefulness in consumer and industrial equipment for frequencies up to 100 Mc and in computers using nonsaturating logic circuits. In all of these applications, the alloy drift-field type is now facing strong competition from both germanium and silicon mesa and planar units.

MADT Types

The drift-field and micro-alloy approaches have also been combined to produce the micro-alloy diffused transistor (MADT). Until recently, these were used extensively in very-high-frequency amplifiers and in very fast low-power switches. Because the intrinsic region thickness of the MADT can be carefully controlled, it works well in saturation. MADT types, like the regular alloy types, have been refined and improved continuously. However, the low power capability of the MADT (which makes it susceptible to burn-out) and its poor mechanical reliability have been disadvantages. Moreover, epitaxial germanium and silicon mesa and planar transistors are now able to compete technically and cost-wise with the MADT in all respects. Therefore, these advanced types appear to be the transistors of the future.

Mesa Transistors

Mesa transistors differ from alloy and alloy-drift transistors in that the starting material is the collector rather than the base. The base of the mesa is diffused into the collector, and the emitter is either diffused or alloyed into the base. A mesa is then etched to reduce the collector area at the base-collector region (Fig. 4).

The mesa structure has several important advantages:

The base width can be very closely controlled, especially when shallow emitter alloying or emitter diffusion is used. With this narrow base width, there is no loss of mechanical strength or power dissipation as in the MADT. The diffused base-collector junction allows a higher voltage breakdown with a given collector resistance. This feature has made the mesa technique invaluable in producing high-voltage transistors.

There are, however, some drawbacks:

Because of need for a base contact, the collector capacitance is larger than that of an MADT having the same emitter size. Also the collector thickness required for mechanical handling purposes produces a voltage drop across the collector and increases the stored charge in saturation. However, developments in the past few years have made the mesa transistor competitive with the MADT in every way and have placed it in a power and reliability class by itself.

Geometry Control of Mesas

Some of the geometry control that permits the collector area and capacitance to be reduced has been accomplished by brute force. As shown in Fig. 4, the alloyed dots have been made smaller for mesas that use alloyed emitters and base contacts. Since the mesa has no line-up problem between the emitter and collector dot, as in the usual alloyed transistor, dot sizes are limited only by the need for making contacts to them; present limits for dot diameters are three or four mils. The mesas are etched right to the edge of these dots to keep the collector capacitance to a minimum. Mesa types with gains up to 20 db at 200 Mc have been made for amplifier applications. Further advances are being actively pursued by the possible use of smaller dots.

Mesas using evaporated emitters and base contacts are shown in Fig. 5; such transistors are limited in area only by the lead attachment problem. Emitters as small as 1 by 2 mils are possible when ½-mil connector wires are used; these mesas provide gains approaching 20 db at 200 Mc. Laboratory units with very small areas have demonstrated appreciable gain in the gigacycle region. Such typical new germanium mesa types as the 2N705 for switching and the 2N700 for amplifiers have become most popular and are rapidly supplanting the MADT for new applications.

Double Diffusion

A more elegant method of controlling base and emitter areas is by masking and double diffusion; a typical p-n-p device is shown in Fig. 6 and an n-p-n in Fig. 7. To date, this method has been carried further with silicon than germanium. The oxide deposit formed by heating silicon to a high temperature masks the transistor against either an n- or a p-type impurity. The oxide can be removed by the usual photoetching techniques in areas where diffusion is required in a base or an emitter. The photoetching techniques have been refined to such an extent that lines 0.1 mil wide can be etched in the oxide, thus permitting emitters and base contact areas as small as the wires that can be attached to them. Amplifier transistors with 1-mil-diameter emitter and base areas of about 2 mils in diameter appear possible. Gains of 20 db at 200 Mc appear easily possible.

The Planar Approach

Other new techniques such as the planar approach open up even greater possibilities; in this method, base diffusion as well as emitter diffusion is from a limited-area source (Fig. 8). The principal advantages of this are greater stability during life, a more constant beta with current, and a very low I_{cbo}. Planar transistors have been found to have a very low noise at very low frequencies ($1/f$ noise) consistent with low I_{cbo}. These features are probably inherent because of the oxide coating of all junctions—something not possible in mesa types. Another advantage of the planar construction is that the metallic coating from the emitter or base contact area can be extended onto the oxide where connections can be made. This approach permits very small active areas with larger areas for the wire contact, a very useful feature for integrated devices.

The planar device, however, has two drawbacks: First, for a given collector area, capacitance is somewhat larger; this disadvantage can be compensated with a slightly reduced geometry. Second, although the low-voltage I_{cbo} is an order of magnitude or more lower with the planar structure, voltage breakdown figures have not been as good as those obtained with mesas having the same crystal resistivity. Processing refinements should dispel this problem.

Silicon vs. Germanium

The use of masking and photoetching has been carried further with silicon than germanium; however, a great deal of work is being done to apply the same approaches to germanium. The planar approach appears to be applicable to both p-n-p and n-p-n germanium structures. Because of the greater carrier mobility in germanium, it is generally thought that germanium would be used for the very highest frequencies. In very-high-frequency structures, however, the input and output capacitances are as important as the mobilities. This fact, along with the better temperature capability of silicon, may make it the logical choice.

Gains of 20 db at 200 Mc are achieved with both silicon and germanium. The noise figure at 200 Mc for germanium is as low as 5 or 6 db; for silicon, it has so far been higher. Germanium has been pushed faster than silicon into the gigacycle ranges, but silicon may overtake germanium. In the next few years, transistors with gains of 20 db at 1 Gc appear feasible in both germanium and silicon. The noise levels obtained may be the determining factor as to which material is used for very-high-frequency low-level amplifiers. For switching, this is not a consideration.

Epitaxial Layers

The second development which has improved the mesa (or planar) approach is the use of epitaxial material. This idea is an old one, but its use in semiconductors is recent. Epitaxial construction permits the growth of a very thin layer of semiconductor material of the desired resistivity. The epitaxial layer need only be thick enough for the needed design parameters of the transistor. The epitaxial approach to a planar transistor is shown in Fig. 8 and to a mesa transistor in Fig. 9. The layers are usually in the range of 0.1 to 0.5 mil. The carrier material, which serves only as a holder, is of such low resistivity that the voltage drop across it and the charge storage in it are negligible. Improvement in the performance of mesa or planar transistors with the epitaxial approach make them completely competitive with the MADT.

Triple Diffusion

Another approach is to use triple diffusion instead of the epitaxial method. Triple diffusion applied to a planar structure is shown in Fig. 10; the collector side of the wafer is diffused to provide a very low resistivity. The triple-diffused method has one drawback; in diffusing the transistor base, it is more difficult to control the top layer thickness of original resistivity. However, triple diffusion has the advantage of producing a top layer with any desired value of resistivity; the epitaxial approach is at present limited to a few ohm-centimeters. The triple-diffused structure, therefore, is applicable for high-voltage transistors, especially for nonsaturated use.

HIGH-POWER TRANSISTORS

As mentioned above, it is not clear whether silicon or germanium will dominate the small-signal and low-power switching fields. However, in most areas of the high-power transistor field, silicon is rapidly becoming the preferred material. Audio-output-amplifier and power-supply-regulator transistors are an exception because of the very low cost of germanium audio power transistors. The initial problem with silicon power transistors was the poor saturation voltage, which made the usual mesa approach unattractive. This problem was solved by transistor designs like the 2N1492, in which the collector and emitter are simultaneously diffused from opposite sides and part of the emitter is etched off to obtain a base contact.

Triple-Diffusion and Epitaxial

The single-diffused approach described above has provided excellent silicon power transistors with low saturation resistances and good reliability. Because of the very low saturation resistance, this approach will be used for a long time. Diffusion from both sides, however, like alloying from both sides in an alloy type, makes control of the base width difficult. The frequency response, therefore, is limited in the single-diffused device. With the advent of triple-diffusion and epitaxial layers, it is now possible to make power devices using the mesa or planar approach, and obtain fairly low saturation resistance and much higher frequency response. Transistors with power outputs of nearly 100 watts at 50 Mc have been designed using triple diffusion. There will be a place both for these and the older single-diffused designs.

Geometry Considerations

Another important factor in the design of high-frequency, high-power devices is the tendency for the emitter to emit only at its edges at high currents, especially in silicon types. Optimum high-frequency results are obtained with the largest emitter perimeter for the smallest emitter area. The shape of the base with respect to the emitter also must be considered, in order to keep the base area and, consequently, the base collector capacitance small, and at the same time keep $r_{bb'}$ low. Good results can be obtained with a variety of geometries, including a ring emitter, a star emitter, and interdigitated emitters and base contacts. An interdigitated emitter design is shown in Fig. 11.

The Future

The field of high-power, high-frequency devices is only beginning to open up. Today, devices are available that will provide 3 watts at 200 Mc, 10 watts at 100 Mc, 50 to 100 watts at 50 Mc, and several hundred watts at 5 Mc. In the next few years, devices capable of several watts at a gigacycle, 50 to 100 watts at 100 to 200 Mc, and several kilowatts at a few megacycles appear to be possible. This area is one of the most exciting in transistor design.

GALLIUM ARSENIDE DEVICES

Other materials, such as gallium arsenide, are also being investigated. From the point of view of temperature capability and carrier mobility, GaAs is the ultimate material; however, in high-frequency transistors it must compete with the refined geometry-control techniques already developed for silicon and germanium. These techniques have not yet been developed for GaAs, but the promise is there. The temperature capability is especially important in the future for microcircuits in which packaging density is very high.

GaAs has found a very substantial place in other areas: In solar cells, its high efficiency together with greater resistance to space radiations make GaAs very suitable. In very-high-frequency parametric diodes, GaAs is an ideal material to achieve the highest-frequency performance. Other areas include GaAs power varactor diodes and GaAs tunnel diodes. In tunnel diodes, life performance has been a problem; however, it appears that this problem limits the use of GaAs in only a few applications.

DIODES AND RECTIFIERS

Although this article has considered mostly one semiconductor device, the transistor, improvements are also being

made in other devices. In power rectifiers, the changes over the last few years have been less revolutionary. The line has broadened, and the reliability has been greatly improved. By stacking junctions, rectifiers can be built to carry several hundred amperes at a few hundred volts, or a few amperes at hundreds of thousands of volts. To date, planar techniques have not been widely used because of the greater difficulty in obtaining high reverse-breakdown voltages. This difficulty will probably be overcome in the near future. Epitaxial layers cannot yet be made of high enough resistivity, but they too offer hope for the future.

However, planar and epitaxial techniques are now being used for silicon signal diodes with great success. The use of planar techniques with signal diodes makes new forms of packaging for these devices possible; junctions are so stable that the usual hermetic package may not be needed. Silicone resins, plastics, and even no encapsulation are being tried. A very attractive approach is the direct sealing of a borasilicate glass directly to the junction. This approach provides both a very small package and a hermetic seal. The planar, passivated surface is needed to withstand the required sealing temperature.

In contrast to the minor changes in the power-rectifier and silicon-diode fields, the semiconductor controlled rectifier is moving very rapidly. Types are available to control currents from a few microamperes to hundreds of amperes. The techniques for controlled rectifiers have tended to follow those of transistors. For the future, all-diffused types (compared to partly alloyed, partly diffused types) will be the most common. The controlled rectifier is rapidly taking over from the vacuum-tube thyratron; with lower prices it will begin to compete against the mechanical switch, and with faster turn-on and turn-off speeds it may compete with the hydrogen thyratron in radar applications.

THE TUNNEL DIODE

Tunnel diodes have not received the widespread use that was predicted for them early in their development. Today, it does not appear that the tunnel diode will ever approach the popularity of the transistor; however, in several applications the tunnel diode is establishing a foothold. As an oscillator or an amplifier at microwave frequencies, for example, the tunnel diode is considerably easier to use than a parametric amplifier which requires a driver; noise level is close to that obtained with a parametric amplifier. For use at higher frequencies and higher power levels, the tunnel-diode package must be redesigned to fit into a microwave circuit and have very-low-inductance leads. Several watts at a few gigacycles may be possible if these changes are incorporated.

Tunnel diodes are also being used for sampling waveforms in very-high-speed oscilloscopes, as level detectors, as pulse discriminators, and for many other special applications. Successful results for diode logic depend upon holding very close tolerances on such tunnel-diode characteristics as the peak current and the peak and forward voltages. Tunnel-diode logic circuits offer shorter delays, several times less than those of transistor circuits. Recent results indicate that logic stage delays of less than 1 μsec are possible; if accent is put on power consumption, a logic stage with a dissipation of about 50 μw can be obtained. Figs. 12 and 13 show the tunnel diode in cross section and in the final package. For computer memories, the tunnel diode offers speeds several times greater than any other semiconductor on the horizon, but higher cost will probably limit use of the tunnel diode to small systems. Very small size and low power consumption of tunnel diodes also make them attractive for integrated electronics.

INTEGRATED DEVICES

Device integration and microcircuitry are the newest and loudest revolutions in the semiconductor field. Already there has been a great deal of talk and many preliminary starts.

The first approach to integrated circuits has been to put two or more semiconductor devices into one package (Fig. 14). For example, a package could include the several diodes and one transistor needed for a *nor* logic gate. The advantages are smaller size (reducing the length of interconnections), lower cost, and greater reliability because of the fewer packages. A variety of devices in a single package are now available, and the list is increasing daily.

The next step is to put the passive devices into the same package. In the past, the circuit designer has generally chosen to keep the active devices at a minimum and use more passive devices because of their low cost. When building microcircuits in one package, however, the semiconductor manufacturer tends to increase the number of active devices (is costs him little to add one with the planar design) and keep the passive components to a minimum. The circuits chosen by the semiconductor manufacturer are often a compromise because of this approach. A long period will elapse before he and the circuit designer get together completely. The microcircuit offers a complete package to the customer; it puts the burden of circuit design and "prove-out" entirely in the supplier's hands. This approach may turn out to be very attractive to small companies that do want to keep their engineering costs at a minimum; it is, however, restrictive in designing an entire computer, where a myriad of small circuit changes may give a better over-all design.

The approaches discussed thus far, although valuable, do not solve the real problem of computer design—*interconnections*. It appears possible that interconnections can be shortened by use of integrated devices or microcircuits. Many microcircuits can be put into one package to permit the logic to be carried out inside a single package. Reliability must be of a very high order, because failure of one element will cause the entire package to be thrown away. Logically, the only real solution to the interconnection problem appears to be the microcircuit approach, where all the functions of a computer are included in two or three packages. Such an elegant solution calls for solving the reliability problem, the problem of removing heat, and others. Many approaches will have to be explored before a satisfactory solution can be obtained.

[*Editor's Note:* see Kihn, this issue for a complete discussion of integrated circuits.]

STANDARDIZATION AHEAD

The rapid pace of device development has made industry-wide standardization of electrical characteristics very difficult. Each manufacturer has attempted to write specifications which emphasize his own technical advantages. This situation has led to a "specification" contest which is very confusing to the customer. This problem will probably continue to exist until the technical revolution slows down.

There has been great progress in one area, however—that of standardization of the mechanical packages or outlines of semiconductor products. Five years ago, there were no accepted industry standards. Today, the bulk of semiconductors are in industry-recognized packages. Outline standardization becomes even more important as we face the challenge of the integrated devices and microcircuits.

SEMICONDUCTOR PLASMAS

Although a plasma is ordinarily synonymous with an ionized gas, this need not be the case. Materials of solid form can contain charges of both signs that behave much like the ionized gas—collections of charges that also can be called plasmas. Studies of semiconductor plasmas have shown unusual effects, similar to gaseous plasmas, that promise to add further to the yet-imprecise knowledge of plasmas, and which may lead to new devices that make use of semiconductor-plasma instabilities to generate oscillations in the millimeter-wave range and even higher.

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IT IS GENERALLY accepted that a plasma is a collection of positively and negatively charged particles, present in approximately equal densities so that overall the collection is approximately neutral. However, this is not sufficient to distinguish the properties of the plasma from those of a collection of charges of one sign alone. At low density, the two would have similar responses to the application of electric and magnetic fields. The distinguishing feature of the plasma is its great resistance to the presence of internal electric fields, i.e., its strong tendency to space charge neutrality. The potential due to space charge at a point inside the plasma decreases exponentially with the distance from the charge. The mean distance over which the fall-off occurs is:

$$\lambda_D = \left(\frac{\varepsilon\varepsilon_0 kT}{2ne^2}\right)^{1/2} = 49\sqrt{\frac{\varepsilon T}{n}}$$

Where: λ_D (in meters) is known as the Debye length, and the sphere which surrounds the charge with this radius is known as the Debye sphere. The Debye length is proportional to the square root of the plasma temperature T and inversely proportional to the square root of the electron density n. The formula is written in the MKS system: e is the electronic charge and $\varepsilon\varepsilon_0$ is the dielectric permittivity of the medium in which the plasma is situated. The numerical expression is useful in evaluating the Debye length, and typical values are given below.

For the plasma to have space charge neutrality in the interior, its dimensions must be large compared to the Debye length. The second half of the definition of a plasma thus requires that the collection of charges must occupy a volume of space containing many Debye spheres.

There are a number of examples other than ionized gases which satisfy these conditions. Negatively-charged electrons and the corresponding positively charged ions in a solid make up a neutral collection, and provided the solid container is large enough, they will have plasma properties. The extrinsic n-type semiconductor is an example of such a plasma. In this case, of course, the ions are tightly bound in the lattice or in some other sites in the crystal. and they behave like particles of approximately infinite mass. The case of holes and negative ions is identical to the first example, and a p-type semiconductor is a good example. Plasmas of these two kinds will be labelled *immobile*, since they cannot be moved or changed in shape without moving or deforming the containing solid.

In addition to the two cases where one of the charged particles is light and the other very heavy, a semiconductor or semimetal may also contain a plasma made up of electrons and holes. An intrinsic semiconductor is an example of this kind of plasma. An electron-hole plasma consists of particles which are all quite light, like the electron. This plasma may be compressed or expanded much more easily in volume than in the case where one of the components is bound into the solid lattice, and it will be called a *mobile* semiconductor plasma.

Before these examples can be called plasmas, they must satisfy the condition that their volume contains many Debye spheres. Intrinsic germanium at 300°K has a density of electrons and holes of about 2×10^{19} per cubic meter and a corresponding Debye length of 10^{-6} meter, a very short distance. At 77°K, fairly pure indium antimonide or extrinsic germanium with electron densities of about 10^{20} per cubic meter have even smaller Debye lengths, 2×10^{-7} meter. Even the low-density plasma in extrinsic germanium at liquid-helium temperature, with its density of electrons and ions of 10^{12} per cubic meter has a Debye length of 5×10^{-4} meter. Certainly, for the first two examples the charge carriers will satisfy the definition for specimens as small as 10 microns. In the last case, the germanium will not contain a plasma if specimens are smaller than about 1 mm.

DR. MAURICE GLICKSMAN studied Engineering Physics at Queen's University, Kingston, Canada during 1946-1949. He received his SM and PhD in Physics from the University of Chicago in 1952 and 1954, respectively. In 1949 and 1950 he worked in the Nuclear Physics section at the Atomic Energy Project, Chalk River, Canada. During 1953-1954 he served as Instructor in the Physics Department, Roosevelt University, Chicago, and in 1954 was a Research Associate in the Institute for Nuclear Studies, University of Chicago. He joined RCA Laboratories as a member of the technical staff in December 1954 and is presently in charge of a group doing plasma-physics research in the Microwave Research Laboratory at Princeton. In addition to earlier work in low-energy nuclear physics and the interactions of elementary particles, his interests have included the measurement of electrical and galvanomagnetic properties of semiconductors and semiconductor alloys, analysis of the problem of ballistic missile defense, the properties of "hot" carriers in semiconductors, the interaction of microwaves with gaseous plasmas, and the properties of electron-hole plasmas in solids. He has received two *RCA Achievement Awards* for outstanding work in research. Dr. Glicksman is a member of Phi Beta Kappa, Sigma Xi and the American Physical Society.

GENERATING SEMICONDUCTOR PLASMAS

It is very easy to make a semiconductor which contains a plasma, either of electrons and ions, or of electrons and holes. There are five different ways to generate a plasma in the semiconductor: heating, DC discharge, RF discharge, injection, and irradiation. Four of these may be used to generate both mobile and immobile semiconductor plasmas.

Heating

First. the plasma may exist in thermal equilibrium. The examples discussed earlier of extrinsic and intrinsic semiconductors fall into this category. In this case. there is no need to add energy to the semiconductor to maintain the plasma. It is thus possible to produce this plasma easily in the laboratory — in contrast to the gaseous case. The difference is of course due to the much smaller ionization energy in the semiconductor. In the extrinsic semiconductor. the energy necessary to ionize the semiconductor impurities is less than the thermal energy, kT. In most cases this is less than 0.01 ev, while for gases the energy necessary is at least of the order of 4 ev. Both mobile and immobile semiconductor plasmas may be produced in thermal equilibrium.

DC Discharge

The second example. the DC discharge, is very familiar in the case of gaseous plasmas and is widely used in gas tubes. lamps, etc. The semiconductor phenomenon involved is often called avalanche ionization, or breakdown. Particles pres-

ent in the semiconductor are accelerated in a high electric field to energies large enough so that they may ionize either impurities in the semiconductor (impurity breakdown), producing an immobile plasma, or the host atoms of the crystal, producing a mobile plasma of electrons and holes. This process may be made to occur in the bulk of a semiconductor crystal, or in the high field region of a junction. Because of the rather large fields required for most semiconductors, the mobile plasma is normally produced in a junction, where the fields of more than 10^7 v/m may be achieved without appreciable difficulties with breakdown in the surrounding atmosphere or on the surface. However, in the semiconductors indium antimonide and indium arsenide, the field necessary for production of an electron-hole plasma is much lower — only of the order of 2×10^4 to 10^5 v/m — and such plasmas have been produced in bulk material. Experiments performed with plasmas produced in this manner will be discussed later.

RF Discharge

The RF discharge is much like the DC discharge, in that an RF field is used to add energy to some carriers initially present, which then are sufficiently energetic to produce a plasma on impact with impurities or the host lattice. Such a technique has been used to make an immobile semiconductor plasma in studies at very low temperatures: it has the advantage of not requiring physical contacts to the material. There is no reason, in principle, why it could not also be used to make a mobile semiconductor plasma.

Injection

In injection, the plasma is made up by adding to the volume the two components, which would be electrons and holes in the case of the semiconductor mobile plasma. These may be injected from appropriate contacts to the semiconductor — a transistor is a good example of a semiconductor containing a plasma of this kind. This technique cannot be used to produce the immobile kind of plasma, since the ions cannot be injected in the usual sense.

Irradiation

The last technique used in the generation of a plasma involves direct irradiation — the addition of energy in another form to the semiconductor to ionize either impurities or the host atoms, and thus produce either the immobile or mobile plasma. Electromagnetic radiation, consisting of photons of energy above the required ionization energy, will produce a pair of plasma particles per photon absorbed when the energy is just above the threshold. Charged particles will ionize the atoms by impact as they traverse the semiconductor, producing many plasma pairs per particle if the material is thick enough.

SIGNIFICANCE OF SEMICONDUCTOR PLASMA PROPERTIES

Plasmas have been made by all five techniques, and their properties have been investigated. In the case of the RF discharge and irradiation, however, it has not been the plasma whose properties were studied, but rather the behavior of the individual carriers in the plasma.

Consider now the properties of the semiconductor plasma which make it of particular interest to the physicist and to the engineer. Of course, just the ability to produce it in a nonequilibrium situation allows some useful devices — e.g., the avalanche diode and the impact ionization diode, which may be used as switches. In this case, the production of the plasma brings with it an increased conductivity, due to the much-increased density of the carriers and not to their plasma character.

In general, the electrons and holes in the semiconductor plasma have a short mean free path; their collision frequency is thus very high (perhaps 1 Tc at room temperature, going down to a few gigacycles at 1°K). Forces which act on the individual electrons thus are quickly distributed to the surroundings through collisions.

Plasma Frequency

The effect of a plasma on an electromagnetic wave may be described in terms of the plasma frequency, i.e., the frequency at which the electrons can describe longitudinal oscillations in the plasma. The well-known expression for this frequency f_p, in cps, is:

$$f_p = \frac{1}{2\pi}\left[\frac{ne^2}{m^*\varepsilon\varepsilon_o}\right]^{1/2} = 8.98\left[\frac{n}{\varepsilon(m^*/m_o)}\right]^{1/2}$$

Where: m^*/m_o = ratio of the mass of the plasma particle to that of the free electron. In general, the carriers in semiconductors behave as if they have masses different from that of the free electron, and most of the known values of m^*/m_o are less than one. For intrinsic germanium at room temperature, the electron plasma frequency is about K-band (27 Gc); for indium antimonide with 10^{20} plasma particles per cubic meter, it is about 225 Gc. These plasmas then have their resonant frequency in the millimeter range, and provide a simple way of getting a plasma with such a high plasma frequency.

The plasma frequency is also a dividing point in the response of a plasma to an electromagnetic wave. At frequencies below the plasma frequency, an incident wave is reflected, while at frequencies above the plasma frequency, the wave is transmitted with some attenuation and phase shift. This simple picture, which works well in describing the gaseous plasma, is more complex in the semiconductor plasma examples because of the normally small size of the semiconductor plasma. At the lower frequencies, then, the semiconductor plasma may be much smaller than the penetration depth of the wave and there can be some penetration and transmission of the electromagnetic signal. When the frequency is high enough, the problem of the small size of the plasma is not present, and plasma densities have been obtained by measurement of the plasma frequency.

Pinching

When a current sufficiently strong is passed through the mobile semiconductor plasma, the plasma will reduce in size because of the pinching force of its self-magnetic field (Fig. 1). At low currents, the electron-hole plasma will occupy the complete volume of the semiconductor, as shown by the dashed lines (Fig. 1) which illustrate the outer surface of a cylinder. There will be a small azimuthal magnetic field due to the current passing through the material. When the current is large enough so that the force it exerts on the current-carrying elements (through its own magnetic field) can exceed the kinetic "pressure" of the plasma, the current will be forced in towards the center, and the cylindrical column of plasma will contract inside the semiconductor. This effect has been observed in a plasma produced by a pulsed discharge in indium antimonide at 77°K. Plasmas with densities in the range 10^{19} to 10^{21} per cubic meter have been pinched down to a radius which was calculated to be as small as about 20 percent of its original value.

An example of the type of observation which is used appears in Fig. 2. The

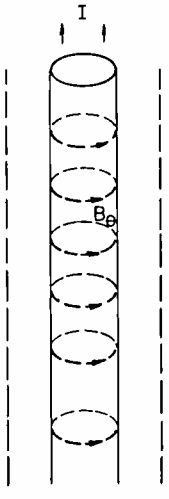

Fig. 1—The electron-hole plasma in a self-pinched condition.

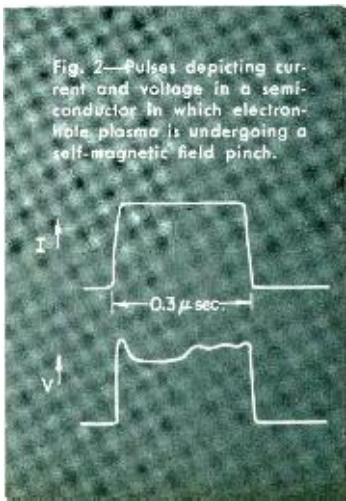

Fig. 2—Pulses depicting current and voltage in a semiconductor in which electron-hole plasma is undergoing a self-magnetic field pinch.

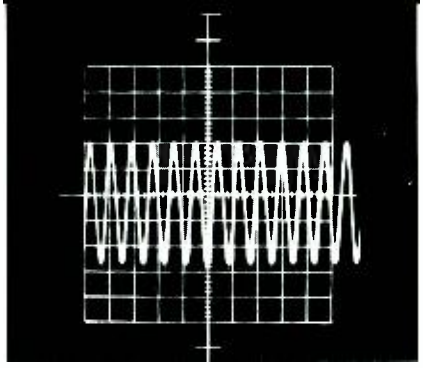

Fig. 3—Current in a 2-Mc oscillistor.

current pulse is displayed above the voltage pulse: the current is derived from a resistor in series with the semiconductor, while the voltage is that across two probes attached along the length of the semiconductor. At low currents, both pulses are identical, and the same as the one shown in the upper sweep. The voltage pulse shown is observed for an intermediate current, well above the threshold for pinching. The circuit is arranged for constant current and the first fall-off of the voltage pulse, right after the initiation, marks the production of the discharge and the plasma. During the relatively flat part of the pulse which follows, the plasma begins its contraction, which is culminated about half-way through the pulse. The oscillations on top of the pulse are somewhat accentuated here; the latter part of the pulse is quite flat. Thus, the plasma in the Fig. 2 case pinches down in about 0.15 μsec, and stays pinched down in cross-section for times as long as at least 1.5 μsec. The functional behavior of the measurable quantities — such as the threshold for pinching, the dependence of the pinch-time on current, and the increased resistance in the pinch — are in good agreement with what is calculated for a pinching plasma. The oscillations on top of the voltage pulse which occur after the pinch is completed are ascribed to hydromagnetic waves induced in the pinching process. The measured frequencies and decay times are in fair agreement with those calculated for such instabilities.

Induced Instability—The Oscillistor

There is another class of instabilities[1-3] in plasmas which was recently discovered. It is interesting that the oscillations were seen independently in both gaseous and semiconductor plasmas, although the workers were unaware of each other's observations for several years. They have been explained theoretically only during the past year. The semiconductor plasma instability was labelled the *Oscillistor* by Larrabee and Steele, who investigated it in some detail.[2] A plasma must be present in the semiconductor: in the first observations, this plasma was produced by synthesis, i.e., injection from contacts. A current and a magnetic field parallel to the current are applied to the plasma. When this occurs, and the values of both the current and the magnetic field are large enough, the plasma exhibits spontaneous oscillations in the current amplitude. These oscillations may be very large (70 percent of the DC current) and persist for long periods. Fig. 3 shows a typical oscillogram of a 1-Mc Oscillistor. Experiments have shown them in the semiconductors germanium, silicon, indium antimonide, and experiments also have shown that they are not due to a negative resistance of the current and voltage, nor to parasitic oscillating tank circuits associated with the crystal contacts, leads, etc. They are thus an intrinsic property of the plasma in the semiconductor. Frequencies observed normally were from 1 kc to 50 Mc.

Fig. 4 shows an idealized geometry with the applied current and magnetic field. The cylindrical geometry is chosen for ease of discussion of the theory. Normally, the plasma will be distributed throughout the semiconductor with a maximum in density at the center and a minimum at the surfaces, where the plasma electrons and holes recombine. However, in the presence of the longitudinal magnetic field, a helical perturbation of the current can be shown to be unstable. The magnetic field acts on the azimuthal perturbed current to increase its radial motion, driving it out to the walls. A theory has been developed for the semiconductor plasma which shows this instability, and predicts the currents and magnetic fields which allow the oscillations to grow. The theory shows that at a given electric field or current, the plasma will be stable until the magnetic field exceeds a calculated threshold value. Above this point, the plasma should become spontaneously unstable. The behavior predicted is in good accord with the observation, as to the form of the behavior on the fields, the rough magnitudes of thresholds and frequencies observed, and the dependence of the various parameters on the dimensions of the plasma. The simplicity of the device can be seen in the photograph (Fig. 5), which shows a germanium oscillistor without the magnet. Magnetic fields of the order of 3000 gauss (or more) are needed to set the current into oscillation.

Applications other than to the obvious AC generator are being investigated. The Computer and Controls Products Section, DEP-ACCD, Burlington, has been studying the feasibility of the Oscillistor as a sensor, e.g. to convert analog (voltage) information into digital (cycles) output, and to convert temperature changes into simple digital information. The attractiveness of the Oscillistor for uses of this kind lies in the threshold character of its response, with the rapid rise of AC output and the very large output signals possible.

Fig. 4—Geometry for theoretical model of an oscillistor.

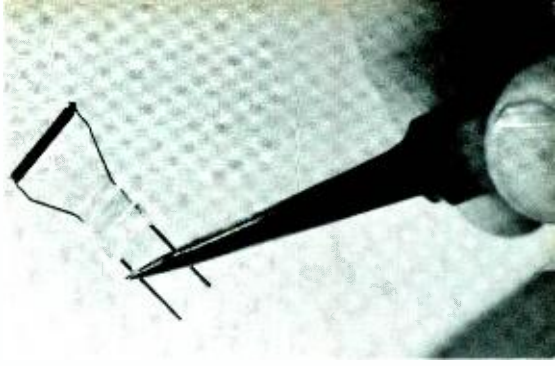

Fig. 5—An oscillistor of germanium, without the magnet which provides the field necessary to set the current into oscillation.

The instabilities discussed above are in the relatively low-frequency range: kilocycle and megacycle. A class of instabilities predicted by Pines and Schrieffer[4] to occur in a plasma with just a current passing through it should be present in the hundreds of gigacycles. These are two-stream instabilities, familiar to engineers working with electron-beam devices, but as yet unobserved in the semiconductor plasma. If found, these could provide a potent new device for producing millimeter waves.

SUMMARY

Most of the scientists who work with semiconductors have been using or studying plasmas, but for most of them, the fact that a plasma was present did not affect the situation. In recent years, studies of these plasmas have shown some unusual effects, similar to those which are seen in gaseous plasmas, and which promise to add further to the yet imprecise knowledge of plasmas.

With what is known of the general properties of plasmas, one can look forward to possible new devices which make use of the higher-frequency instabilities to produce oscillations in the millimeter-wave range and even higher.

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INTEGRATED ELECTRONICS ...A Survey

Developments in integrated electronics will profoundly affect the design of electronic devices and systems, and their maintenance procedures, before the end of the 1960's. It is important that RCA product engineers stay abreast of this field and seriously consider its philosophy and the new techniques that flow from it in designing future systems and hardware. This paper reviews and evaluates several significant current approaches. To further assist the engineer in gaining more-detailed information, a selected bibliography of over 50 significant literature references is included, extracted from the extensive bibliographies on this field prepared by the RCA Integrated Electronics Committee, which also recently sponsored an RCA Symposium on the subject.

H. KIHN, Staff Engineer
(Chairman, RCA Corporate Integrated Electronics Committee)
Research & Engineering, Princeton, N. J.

HARRY KIHN received his BSEE from The Cooper Union Institute of Technology in 1934, and his MS from the University of Pennsylvania in 1952. Mr. Kihn joined RCA in 1939 as a research engineer associated with television receiver and circuitry development. During World War II, as a member of the technical staff of RCA Laboratories at Princeton, he performed research relating to radar for automatic bombing and altimeters. With the advent of color television development in the post-war period, he played a prominent part in the development of receiver circuitry. Subsequently he was engaged in further radar research and directed research in pulse code and digital communication and computer systems. Since early 1960, he has been a Staff Engineer on the RCA Research and Engineering Staff, in charge of coordinating RCA technical activities in data processing and semiconductor devices, including both defense and commercial applications. He has recently been serving as Chairman of the RCA Integrated Electronics Committee. He is a *Fellow* of the IRE, and is a Member of Sigma Xi, and the AIEE.

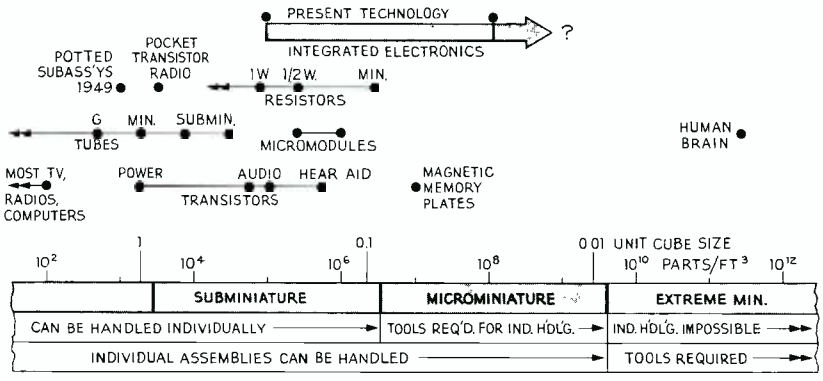


Fig. 1—The trend in size and packaging density.

Table I—Integrated Electronics Techniques Now Under Active Industry Development

1. *Micromodule*[5,6] or 3D stacked individual (and some multiple) component wafers.
2. *Microcircuit*[7] (or 2D circuit) incorporating flat, plated or evaporated and thin-film active and passive components as complete circuits.
3. *Silicon semiconductor circuits*[8] which utilize characteristics of doped materials to perform active and passive circuit and subsystem functions (functional blocks).
4. *Molecular circuits*[9] which seek to accomplish a complex electronic function by physical phenomena in a material.
5. *Direct-coupled transistor-logic circuits*,[10] specialized computer circuits involving multiple transistor-resistor technology packaged in a transistor case;
6. *DCUTL circuits*[3] consisting of direct coupled unipolar transistors as logical and switching elements;
7. *Solid ceramic circuits*[11] incorporating passive circuitry imbedded in layers of thin ceramic wafers fused into a synthetic laminar solid with multiple active devices incorporated in the complete package.

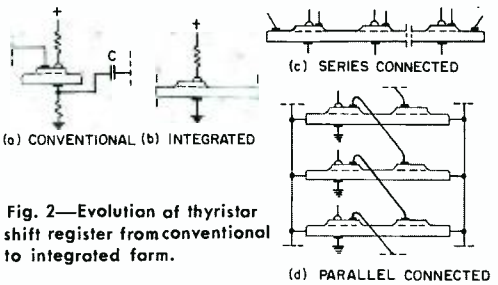
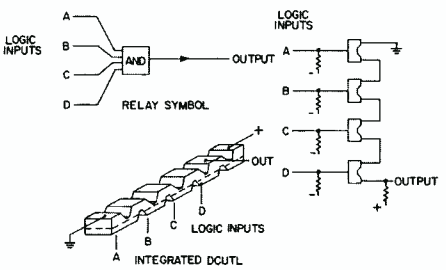


Fig. 2—Evolution of thyristor shift register from conventional to integrated form.

Fig. 3—Multiple and-circuit DCUTL of four active and one passive unipolar elements.



ELECTRONICS IS EXPERIENCING a revolution in the design and packaging of circuits and subsystems—the development of microsystems. The frontier area of microsystems is *integrated electronics*, which combines solid-state devices with sophisticated systems concepts to provide optimum-size combinations of functions that most efficiently meet system requirements. The solid-state devices may be semiconductor, magnetic, cryogenic, optoelectronic, ceramic, etc. The system requirements involve reliability, performance, initial and maintenance costs, power density limitations, and physical size and weight.

Fig. 1 shows the trend of component and circuit miniaturization.[1] Integrated electronics, by our definition, covers a broad spectrum from 10^5 parts/ft^3 to an undefined upper limit—presently bounded by fabrication technology and power density limitations to approximately 10^8 parts/ft^3.

An early concept of integrated electronics completely disassociated itself from discrete components. It proposed that fundamental physical phenomena be adapted to function—not as single components, but rather as integrated circuit aggregates to perform complete electronic tasks. The shift-register transistor[2] based on the thyristor principle, the direct-coupled unipolar-transistor logic (DCUTL)[3], and the semiconductor delay lines[4] are examples. Herein, several different device mechanisms are integrated into a single piece of semiconductor, whereby certain portions of the unit serve as circuit connections. Practical implementation of this approach still incorporates distinguishable component functions, but the reduction of equipment size is several orders of magnitude compared to the most advanced miniaturization schemes in current use.

A both more immediate and realistic approach to integrated electronics is to consider it as a combination of discrete deposited or otherwise-fabricated active and passive elements on a substrate that minimizes the number of internal and external interconnections, with optimum

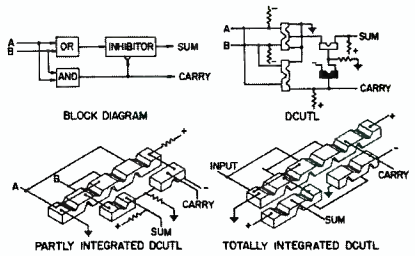


Fig. 4—Evolution of a conventional half adder to a completely integrated DCUTL device.

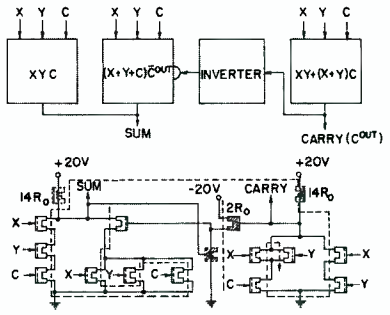


Fig. 5—Evolution of integrated full adder using unipolar transistors.

Fig. 6—Ceramic micromodule-wafer implementation of full adder (0.31-inch square, volume, 1/400 cubic inch).

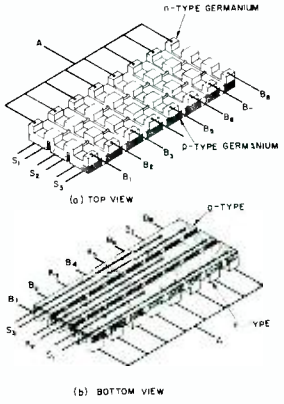


Fig. 7—Computer transfer tree in proposed integrated form.

encapsulation techniques to protect the resulting integrated device against environmental influences. This approach is now being taken by nearly all the companies active in the field.

Since we are here mainly concerned with new devices and those which will come into fruition during the decade, the spectrum of miniaturization dealt with herein will lie between 10^5 and 10^7 parts/ft^3. These ground rules eliminate cordwood, macromodule, weld-stick, minimodule, and similar techniques (now in production) which utilize compactly packaged conventional components. Also not discussed are early efforts at microminiaturization such as the megacoder[12] and the microminiature PPM system[13]. Although these devices still utilized discrete-component packages in a unique manner, they integrated novel systems and circuit concepts with effective microminiaturization as a goal.

Several approaches to integrated circuits which fit into this spectrum are under active development in the electronics industry and are listed in Table I.

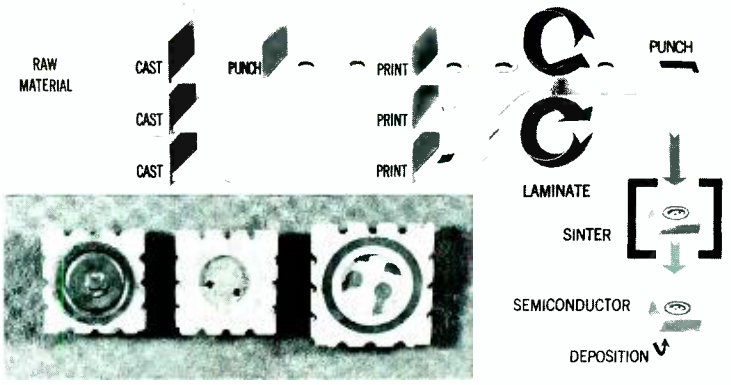


Fig. 8—The new RCA solid-ceramic circuit. The wafers shown are: left, unfired state with all passive elements plus interconnections between ceramic layers; center, after firing, with a transistor and diode pellet mounted in the cavity; right, active elements sealed in ready for use.

MICROMODULES—THE FIRST MAJOR STEP

The first major step in the microminiaturization process, wherein *the components were tailored for integration*, was the RCA micromodule program[5,6] (under Signal Corps sponsorship). It attains component densities of approximately a half million per cubic foot.

DEP is making extensive use of micromodules in many programs, including MICROPAC Computer, the AN/PRC-51 Tactical Field Communications equipment, Inertial Guidance Platform Circuitry, and Infrared Seeker Equipment. Also, RCA is now marketing micromodules commercially, as well as in the form of a Micromodule Laboratory Kit, through the Semiconductor & Materials Division.

While the original micromodule concept involved a one-to-one correspondence between its wafers and conventional components, the micromodular technique has since developed automatable substrates, and there are many sophisticated *integrated* devices, semiconductor circuits, and similar structures that can be incorporated *with a wafer as a supporting member*. It can easily acomplish a complete circuit per wafer, through both evaporative deposition and masking, and by alloying, diffusion, and epitaxial growth of semiconductor active elements.

This program is of great importance both to RCA and the military services, since it is *the only technique* which has promise of large-scale, high-reliability production in the immediate future. [*Editor's Note:* see also papers by Szukalski, Leshner, and DiStefano (including his bibliography), in this issue.]

INTEGRATED SEMICONDUCTOR DEVICES

Almost simultaneous with micromodule development was the work of the RCA Laboratories incorporating active and passive components in a single piece of semiconductor material with substantially no interconnecting leads. The basic active elements used in the integrated device circuitry were the thyristor[2] and unipolar transistors[11,15,16].

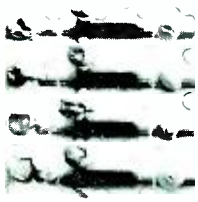


Fig. 9—Array of four thin-film field-effect-transistor triodes deposited simultaneously on a ceramic wafer used in the solid-ceramic-circuit package.

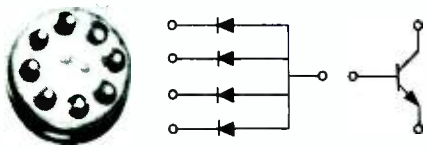


Fig. 10—Mutiple-active-device package: a diode transistor gate. Similar examples include a diode gate, isolated transistors, and a Darlington circuit.

Fig. 11—Prototype ferrite operture plate memory less than 1 inch square. Array of 16 x 16 holes, 0.025-inch diometer, on 0.050-inch centers.

Fig. 12—Metollic etched-sheet memory.

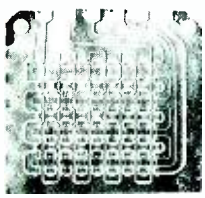


Fig. 13—Cryoelectric film-matrix memory.

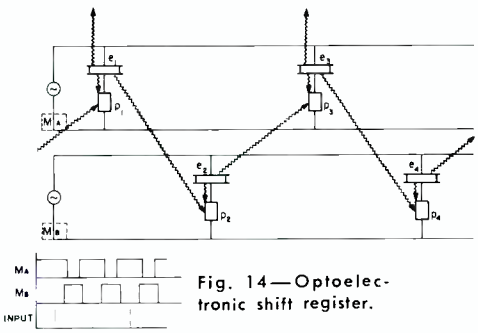


Fig. 14—Optoelectronic shift register.

Thyristor Shift Register

The thyristor is a transistor which behaves much like a thyratron and is capable of being triggered *on* and *off* by low power. Because of a negative-resistance characteristic within a well-defined range of current and voltage, it may be used as a bistable element to store one bit of information.

One stage of a thyristor shift register depicting the evolution from a conventional to an integrated circuit is shown in Fig. 2, a typical monostable flip-flop in which the low-current state is the stable state. In Fig. 2b, the RC circuit has been replaced by a semiconductor delay line consisting of a small bar of germanium. The shift pulse is applied along this bar and sends minority carriers from the *on* stage down the bar. These minority carriers are collected at the end of the bar, delayed by the transit time, and serve to trigger *on* the next stage. The complete shift register may take the series or parallel forms shown in Figs. 2c and 2d.

Unipolar-Transistor Integrated Arrays

The unipolar transistor lends itself to very efficient iterative integrated arrays. The unipolar transistor is, in effect, a voltage-controlled relay and may be used in this manner in logic circuitry.

Recent developments in unipolar technology at the Semiconductor and Materials Division utilizing modern deposited films and planar construction, has produced devices of high transconductance, low leakage, current, and low capacity—the important parameters in successful integrated circuitry. This accomplishment will make feasible and available to the equipment designer the following kinds of integrated devices.

DCUTL Multiple And-Circuit

A number of experimental integrated devices utilizing the unipolar transistor in a direct-coupled form, the DCUTL, have been constructed. One of these (Fig. 3) represents a multiple *and* circuit of four active and one passive unipolar elements, the latter as the load resistor. When no signal is applied to the gate inputs, all gates attain a large negative voltage, shutting off all elements. When one or more gates are driven to a less-negative voltage, the corresponding channel resistance shift from high to low value, turning *on* the elements. However, the output voltage will remain highly positive until all the gates are biased to a small negative voltage. In this case, the output voltage becomes a small positive voltage corresponding to *on*.

In many logical structures, alternate elements can have complementary symmetry; i.e., n-type base elements alternate with p-type base elements, and the voltage polarity alternates. This keeps the junctions reverse-biased at all times and requires no cascading of voltage sources.

Integrated Binary Half- and Full-Adders

Another important logic circuit is the half-adder. This circuit adds two digits in the form of *on* or *off* (*1* or *0*) pulses supplied to two inputs and then delivers their sum-and-carry as two output pulses. Such a function is conventionally performed by a score of transistors, resistors, and capacitors. Fig. 4 shows the evolution of a conventional half-adder to a completely integrated DCUTL device—three small pieces of silicon treated to form several active and passive unipolar elements mounted on a thin ceramic wafer that incorporates printed-circuit connection between the elements and power supply.

A further development of this technique is the binary full-adder[17], a computer circuit that adds three binary numbers (*X*, *Y*, and a carry *C*) from a previous stage, giving two outputs—one for the sum and one for the carry to the next stage. The design was first developed in terms of conventional circuitry, and then extended to an integrated module using unipolar transistors (Fig. 5). Four elements in Fig. 5 are different from the rest; two p-type units and two load resistors. These load resistors are unipolar transistors with channels 4.5 times as long as the regular units. The topology of the circuit is such that a continuous path exists through the channels of all the n-type units (dashed line, Fig. 5) allowing the unipolar transistors to be arranged in one row. Thereafter, the metallic connections between adjacent units are replaced by semiconductor bridges. The p-type units are handled in similar fashion. In this form, there are still some connections between elements that are not adjacent. The art of integration is the finding of a circuit layout where these connections are as short and direct as possible. These connections are made by printed circuits on ceramic micromodule wafers, and the semiconductor sticks are soldered directly to these printed circuits (Fig. 6)—an integrated full-adder in 1/400 in^3.

Computer Transfer Tree

A computer transfer tree is shown in a proposed integrated form in Fig. 7. This unit, used to address different parts of a computer memory, is made of 24 unipolar elements connected in eight rows of three elements each. The gates of the unipolar transistors are connected to three flip-flop circuits (not shown) which apply large negative bias to the gates corresponding to *off*, while the other gates are given a small negative bias corresponding to *on*. Therefore, only one row of unipolar elements will be all *on*, connecting the input to one of the outputs. The other rows will have at least one element in the *off* condition, thus disconnecting all other outputs.

Future Potential

Entire logic portions of a digital computer may contain nothing but integrated devices in which small silicon elements or other type of unipolar device are sandwiched between ceramic insulating wafers and the sandwiches stacked. The fuller implementation of this approach in the future has been enhanced by recent progress made in planar unipolar-transistor fabrication in recent months as well as the development of the thin-film-transistor techniques to be described later.

SOLID CERAMIC CIRCUITS

While the above integrated-circuit developments were being carried on in the RCA Laboratories, another approach was being followed in the Semiconductor & Materials Division, as an outgrowth of the ceramic technology developed in the micromodule program. This solid-ceramic-module technique (Fig. 8) involves the fabrication of large-area ceramic sheets, which can have thicknesses of 0.002 inch or less. While in the unfired (green) state, these sheets can be punched, printed, and otherwise manipulated to form arrays of interconnected passive circuitry. When successive layers are stacked and fired, a monolithic, hermetically sealed, interconnected block of passive circuitry is formed. The module is completed when active semiconductor components are subsequently sealed in the end cavity.

The active components incorporated in this monolithic ceramic package can be the best combination of single, multiple, or integrated devices that satisfies the performance and economic aspects of the desired application. Such capability of combination between passive and active components gives this approach an applications flexibility lacking in many other microelectronic approaches.

The planar dimensions of the wafers can be the same as a micromodule wafer, *but the depth is at least an order of magnitude smaller* than the equivalent micromodule circuit or subsystem, with a considerable reduction in the external interconnections required.

Many of the techniques developed under the micromodule program are used in the application of the printed circuitry

to the wafers, thus giving promise of eventually high-speed, automatic manufacture of both the wafers and the completed subsystem module. Inductive as well as capacitative wafers have been developed to allow a wider range of circuit combinations to meet the requirements of both digital and analog circuitry. Because of the use of ceramic substrates, temperatures considerably above that allowable for germanium and silicon can be tolerated, and the position of the heat-source wafers can be arranged so as to lie at or near the outside surface of the module, thus minimizing internal hot spots.

This approach is truly a synthetic integrated circuit, because after processing, the individual wafers have lost their identity and the circuit elements and their interconnections are truly contained *within* the homogeneous solid. *The solid-ceramic circuit is thus a logical successor to the micromodule technique in future microminiaturization.*

Computer inverter circuits have already been fabricated and pilot production of a number of similar circuits will be realized during 1962. It is sufficiently flexible and versatile to encompass both digital and non-digital circuitry, as well as thin-film circuits including the new thin-film transistors.

THIN-FILM DEVICES

In addition to the techniques described above, work on thin-film phenomena, active and passive, has been carried on by RCA Laboratories, DEP Applied Research, the Electron Tube Division, and Electronic Data Processing.

Thin films are sometimes considered a fourth state of matter, since they often have properties different from the bulk material, depending on their thickness (which may range from less than 100 angstroms to approximately 10,000 angstroms). They serve as interconnections, (thick films of gold, aluminum, copper, platinum); as resistance, (nickel, metal alloys, tantalum, tin oxide); as capacitance (tantalum oxide, ceramic films); and as inductance (spiral conductor films on ceramic substrates or ferrite substrates). Magnetic films for memories (iron-nickel), ferroelectric films, semiconductor films (Ge, Si, CdS, etc.), and cryoelectric films (Sn, Pb, Nb) are other important applications.

Although films have been widely used in fabrication of such passive circuitry and components,[7,18] the absence of an active device which could simultaneously be deposited in large numbers along with the passive circuitry has heretofore hindered greater utilization of this technique. Diodes and transistors had to be inserted onto the substrate (glass or ceramic) which supported the passive thin-film circuitry.

Now, with the recent development of the new thin-film triodes and diodes by the RCA Laboratories,[19] this bottleneck has been eliminated and an upsurge in the thin-film integrated circuitry can be expected. Although this development holds forth the possibility of large-scale deposition of active as well as passive elements so ideal for computer technology, further research is being carried on to ascertain all the parameters affecting the yield and reliability of the devices. [*Editor's Note:* See Weimer, this issue.]

It is worth noting that gains of 40 db and cut-off frequencies of 20 Mc have been obtained to date. This device offers the hope of high input impedance and low-power-level operation so advantageous in high-density packaging of microelectronic parts. It may be feasible to replace individual semiconductor chips in solid-ceramic circuits with evaporated transistors and diodes (Fig. 9).

The possibility of depositing and interconnecting thin-film switching devices in arrays containing several thousand elements per square inch should be realized in the future. Since they will all be fabricated simultaneously, with as few as four evaporation steps, one may anticipate a radical reduction in cost per element.

SILICON SEMICONDUCTOR CIRCUITS

In this technique,[8] a bar of silicon is used as a substrate and active device (diodes and transistors) are fabricated at the desired locations on the silicon bars, usually as multiple planar devices.

In early versions of this approach, as an attempt to justify the concept of "molecular" circuits (all active and passive functions within the solid bar) capacitors were made by back-biased semiconductor junctions, and resistors by the bulk resistivity in properly shaped portions of the silicon bar. Frequency-selective circuits, in the absence of inductance, were obtained by RC networks using feedback around transistor amplifiers.

Because of the difficulty of attaining the correct range of resistance and the sensitivity of the capacitors to voltage and temperature, this approach has been largely abandoned. The present technique involves a silicon substrate upon which the active diodes and transistors are fabricated, with passive components and interconnections deposited upon an insulating film. The latter is usually silicon monoxide made by oxidizing the silicon surface itself at the desired areas. The passive components are generally evaporated films of materials. Interconnections are evaporated through the proper masks in a sequential manner until the complete circuit has been deposited.

This technique has demonstrated considerable success, but has disadvantages: 1) the basic limitation of silicon (a semiconductor) as a substrate, 2) the shortcoming of a completely sequential process where a partial or complete failure at a late stage in the process ruins the whole device, and 3) the inflexibility of not being able to substitute newly developed active devices in a semistandard passive package without changing the whole processing procedure.

In this respect, the solid-ceramic-circuit, multiple-active-device approach is much more flexible because of its parallel processing. The yield and cost problem is dependent for its solution on considerable improvement in the technology of fabrication, particularly automation of the sequential processes of evaporation and masking.

DIRECT-COUPLED TRANSISTOR LOGIC

Here, the same technique is used as in silicon semiconductor circuits, with the substitution of active for passive devices except for one or more resistors.[10] Capacitors thus are eliminated, and advantages is taken of the ease of fabrication of identical transistors on a silicon wafer.

The limitations are 1) the need of much more complex circuitry for a given system function, 2) the inflexibility of limited useful voltage ranges and logic configurations, and 3) the sensitivity to noise when used in a high noise environment as in digital computers for which these specialized circuits were designed.

However, at least six packaged logic functions have been announced and only experience will show how useful this approach will prove.

MOLECULAR CIRCUITS

As far as molecular circuits are concerned, it is too early in the state-of-the-art to expect meaningful advances. The present so-called molecular circuits are identical with silicon semiconductor circuits. True molecular circuits that accomplish a complex electronic function (such as an IF strip) without recognizable components, *have not yet been attained.* A piezo-electric crystal and a semiconductor delay line are examples of this type of circuit. Extensive research in materials and phenomena must precede any practical implementation.

MULTIPLE DIODE AND TRANSISTOR PACKAGES

An important class of semiconductor integrated circuits is the multiple diode

and transistor[20] packaged circuits which the industry and the Semiconductor & Materials Division is developing and fabricating, largely for computer use. Although not so glamorous as the three just discussed, this class of device—particularly the multiple diode—is now making a valuable contribution to the simplification and improved performance of our advanced computers (Fig. 10).

TUNNEL AND VARACTOR DIODE PACKAGES

An increasingly important package approach is the integration of circuit and semiconductor devices in the microwave region to offset the inherent parasitic reactances associated with discrete components and devices, and thus attain wide band highly efficient amplifiers and frequency converters, as well as oscillators. Tunnel and varactor diodes perform the function of active devices in this class of integrated circuits[21,22] which the Microwave Advanced Development Group of the Electron Tube Division are developing. Semiconductor diodes with line and ring junctions, diodes built directly into passive circuits, and the incorporation of both active and passive devices on the same semiconductor wafer are important aspects of this approach.

SEMICONDUCTOR DELAY LINES

The semiconductor delay line, which utilizes excess minority carrier propagation in semiconductors to provide electronically variable time delays, is an ideal integrated device. It combines in a very small volume (10^{-4} in^3) the functions of a lumped-circuit delay line and a voltage-controlled multielement tapped switch. Problems of waveform distortion and signal loss for large delays have not been completely solved, but its utility for delay equalization, tunable amplifiers, frequency modulators, etc., justifies additional research. [*Editor's Note:* See Sein and Levine, this issue.]

INTEGRATED MEMORIES

To this point, the discussion has concerned itself with integrated circuits. Of equal importance are integrated memories for large-capacity random access in computer systems.

In computer applications, arrays of individual cores have become the classical solution for the selective-access high-speed memory chiefly because they have proven to be much more reliable than previously used systems. Memories with hundreds of thousands of individual cores and some with millions are in use. For these and still-larger capacities, it became evident some years ago that the technique of individual cores for this size memory was uneconomical. Considerable research to uncover other magnetic elements has been undertaken.

Ferrite Apertured Plate

The ferrite apertured plate memory[23] was one of the earlier devices developed for this purpose (Fig. 11). This is a plate with a regular array of holes, molded from square-hysteresis-loop ferrite material. The direction of remanent magnetization around each aperture stores one bit of information. There is no interference between magnetizations around adjacent apertures, because for a given current through an aperture, the magnetizing force diminishes gradually with radial distance and, at a well-defined distance chosen to be less than half the width of the leg between adjacent apertures, becomes smaller than the threshold of switchover.

The plate thus constitutes a unit conveniently fabricated as a whole (in a single step) and that is equivalent to a number of cores. Furthermore, since the ferrite is an insulator, it is possible to "print" windings directly on the plate and thereby eliminate the need for some of the manual threading—particularly suitable for making a winding that links all the holes in series.

Magnetic Thin-Film Matrix

The magnetic thin film memory[24] consists of a 20/80-percent permalloy magnetic film deposited on a glass or aluminum substrate, either in the form of discrete islands or as a uniform film, with the deposited coordinate conductors separated sufficiently to isolate the magnetic fields of adjacent bits.

This device is still technology-limited in providing uniform and small-tolerance magnetic properties over a large surface, but this limitation is being rapidly improved. The major shortcoming is, however, the small signal output due to the open magnetic path involved. Even so, the high-speed storage and retrieval, and the advantage of simultaneous deposition and ambient-temperature operation still makes this approach attractive for certain kinds of medium-capacity, fast, potentially low-cost memories.

Metallic Etched-Sheet

The metallic etched-sheet memory[25] (Fig. 12) is an RCA development in which a relatively thick permalloy sheet is etched to provide a matrix of holes about which the circumferential magnetic fields are stored. Deposited through suitable masks upon an insulating layer on the sheet, in proper orientation to the holes, are several layers of conductive windings. Because these windings pass through the holes, thus utilizing a closed magnetic path, the signal level is an order of magnitude greater than that in the thin-film memory. Excellent performance over an unusually large temperature range makes this very useful for space and military use. An important DEP program is based on this technique.

Cryoelectric Film-Matrix

The cryoelectric technique is the most suitable for memory storage capacity in excess of millions of bits (Fig. 13).[26] At temperatures in the vicinity of 5°K, the superconductivity characteristics of lead and tin are utilized to obtain persistent currents that can be turned on and off by the presence or absence of localized magnetic fields. The films of the two metals, as well as insulating films, are fabricated in much the same manner as the thin-film integrated circuits; hence, successful memories are largely dependent on the state of technology of deposition of uniform metallic films, and films which will adhere to a substrate when immersed in liquid helium (the refrigerant). [*Editor's Note:* See Boornard and McEvoy, this issue.]

OPTOELECTRONIC INTEGRATED DEVICES

A new approach to display devices, logic networks, and computer components is the application of optoelectronic[27] elements to shift registers, *and* or *or* circuits, adders, and logical trees.

An optoelectronic element may be defined as a combination of a photoconductor (such as cadmium sulfide) whose resistance is a function of ambient illumination and an electroluminescent cell or electroluminor (zinc sulfide or selenide) which emits light by direct application of an electric voltage. The light amplifier[28] is an important development using an integrated structure of optoelectronic elements. Fig. 14 is a schematic of an optoelectronic shift register which uses photons or light energy as information carriers and electrons for coupling between the electroluminor and photoconductors.

It is evident that the light emission of the electroluminor depends on the presence of photon illumination on the photoconductor. If, in addition, the photoconductor is exposed to the light output from the electroluminor (light feedback), the circuit will remain activated even when the input illumination is removed. This "latching" action requires a proper time constant in the recovery of the photoconductor after the input is removed. Individual elements can be made extremely small and densely packed.

The use of masked deposition, light-

absorbing and reflecting coating, and evaporated conductive films allows the assembly of large number of low-power-consuming elements into computer, visual-display, and light-intensifier devices and systems. The major shortcoming is the slow response compared to semiconductor and magnetic integrated devices, but the capability of simultaneous visual display will insure a fruitful field for optoelectronic microsystems when technological improvements have attained low-cost devices.

IN CONCLUSION . . .

One of the major challenges to the circuit and systems designers in this decade will be the efficient utilization of the integrated-electronics structures resulting from these techniques. Mention was made of RCA defense equipment utilizing micromodular construction; in addition, a miniature computer using silicon semiconductor logic circuits has been demonstrated by the Air Force in a recent public release. But we are only at the threshold.

. . . The Future Trend

If we may predict the trends in this field, the systems designers will probably have available, in addition to the circuits described above, modules capable of flexible logic, low-cost arrays of active elements with prescribed interconnections, and arrays containing imperfections which will produce operable performance by redundant and statistical interconnections. Elements or connections capable of adaptation may become important toward the end of the 1960's. Systems which simulate biological networks will have been developed well beyond the research stage. The present catalog of circuits which perform desired electronic functions will be improved and simplified, resulting in a minimum of functional duplication.

From a systems point of view, the selection of circuits requiring the least number of realizable components, capable of operating under wide tolerances and in simplified modes (such as the digital) is as important as the novel techniques previously discussed in insuring the lowest cost and most reliable microelectronics system of the future.

. . . A Caution for the Present

It is wise, however, in evaluating the various techniques described herein not to abandon completely the accumulated technology of the present for the technical sophistication of the future—unless we are willing to gamble that the five-year (or-more) gap between research devices and their mass-produced, low-cost, highly-reliable ultimate counterparts will not seriously affect the performance of our electronic equipment.

. . . The Long-Run Challenge

In the long run, nevertheless, systems of great complexity, information-handling capacity, and speed, such as the generation beyond the 603 computer, will come to depend on some form of integrated electronics to attain optimum performance parameters. Our engineers and scientists are now evaluating and implementing those circuits most amenable to integration for our advance computers and miniature equipment.

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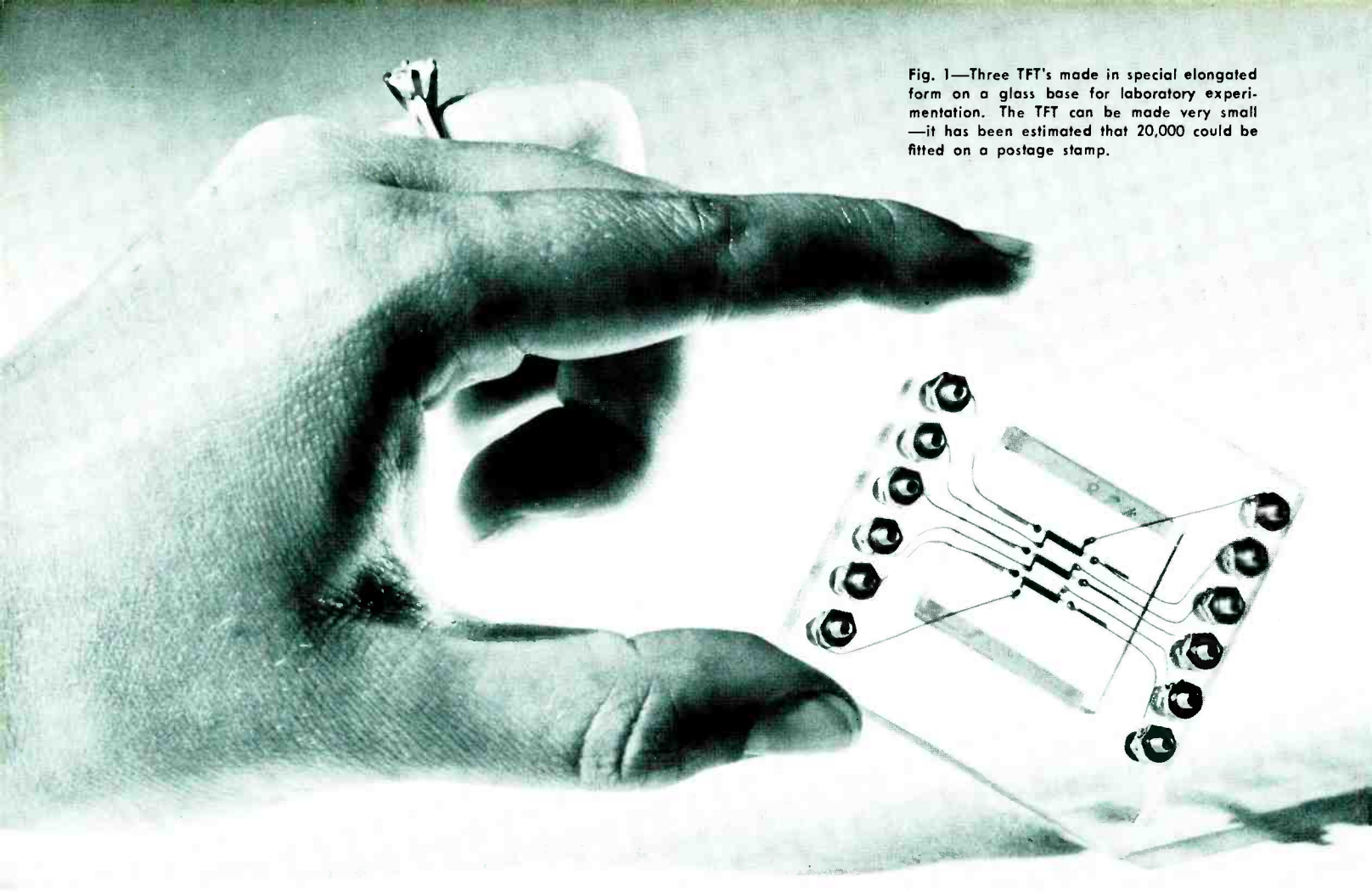

Fig. 1—Three TFT's made in special elongated form on a glass base for laboratory experimentation. The TFT can be made very small—it has been estimated that 20,000 could be fitted on a postage stamp.

The TFT ... A New Thin-Film Transistor

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The TFT is a state-of-the-art advance in thin-film devices, with important implications for integrated circuitry. The same evaporation techniques that produce the TFT allow fabrication of complete functional circuits of hundreds, perhaps thousands, of active and passive components in one operation—including interconnections. Experimental TFT's using microcrystalline layers of CdS have yielded voltage amplification factors greater than 100, transconductances greater than 10,000 μmho, input impedances greater than 1 megohm shunted by 50 pf, gain-bandwidth products greater than 10 Mc, and switching speeds less than 0.1 μsec. Simple evaporated thin-film circuits using the TFT have been built, including a multistage thin-film amplifier. Modified forms of the TFT have been built for use as a flip-flop, AND-gate, and NOR-gate for computer applications.

THE POTENTIAL advantages of thin-film circuits have been largely unrealized because of the lack of a thin-film transistor which could be deposited by the same techniques upon an insulating substrate. The new high-gain transistor described here—the TFT—has all components, including the semiconductor and metal electrodes, deposited by evaporation upon a glass plate (Fig. 1). The word *transistor* is used in its broadest sense here; the mode of operation of the TFT is different from either the conventional unipolar or bipolar transistor.

Performance of the TFT, utilizing microcrystalline layers of CdS, approaches that of commercial transistors made of single-crystal germanium or silicon.[1] The surprisingly good performance of the TFT is partly due to evaporation techniques that permit very small electrode spacings and gate widths. More important, however, has been the development of an insulating gate contact that permits operation in either the enrichment or depletion mode without drawing appreciable gate current.

The enrichment mode is of particular interest from the standpoint of thin-film

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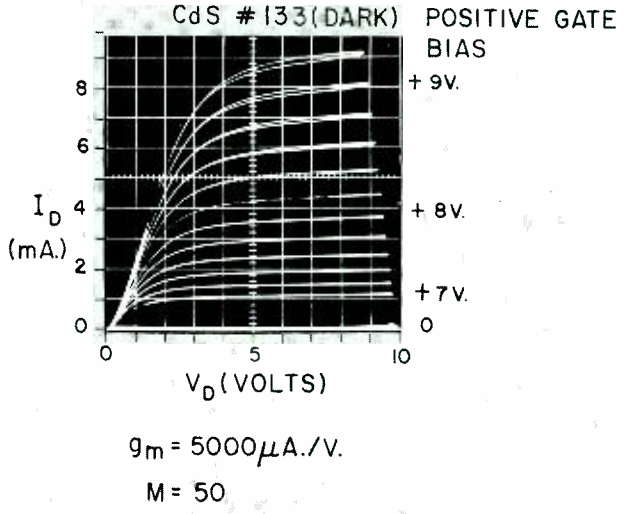


Fig. 2—Characteristic curves for an experimental field-effect triode operating in the enrichment mode. Drain voltage is plotted against drain current for different values of gate bias (source is grounded).

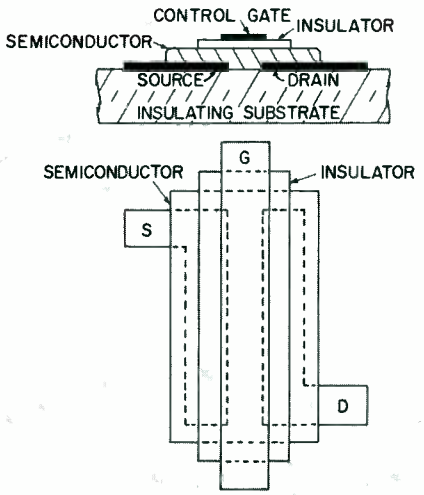


Fig. 3—Cross-sectional and plan view of an insulated-gate TFT. Thickness of evaporated layers are shown greatly exaggerated compared to the lateral dimensions and to the thickness of the sub-strate. Semiconductor thickness may be less than a micron.

circuits, since it permits *direct coupling between stages*. This mode of operation has not been used to date in commercially available transistors, although the effect itself was noted in some early experiments elsewhere. Recently, several experimental single crystal devices utilizing the enrichment effect have also been reported.

Fig. 2 shows a typical set of operating characteristics for a TFT operating in the enrichment mode. Although the curves resemble those of a tube pentode or a unipolar field-effect transistor, a striking difference is noted in the choice of control gate bias.

FABRICATION

Fig. 3 shows one form of insulated-gate TFT. The electrodes, insulator, and semiconductor are deposited by evaporation in successive layers on to a glass substrate. The semiconductor can be of relatively wide bandgap, into which majority carriers are injected from the source electrode.[2] Although microcrystalline films of CdS were used for obtaining experimental measurements, other materials having higher mobility should be applicable as well.

The thin insulator film separating the control gate from the semiconductor permits a mode of operation quite different from that of the conventional field-effect transistor.[3] By biasing the gate positively with respect to the source, the drain current can be enhanced by several orders of magnitude without drawing appreciable gate current. Although negative-bias operation is also possible, the enhancement mode offers a significant practical advantage: direct coupling between stages becomes feasible, greatly simplifying the connections in evaporated thin-film circuits.

The mechanical masking techniques used for depositing the metal electrodes and semiconducting layers in the TFT's are equally well suited for depositing diodes and the passive elements in thin-film circuits. Electrode spacings of less than five microns are readily achieved. Close spacings are desirable in the TFT, since it can be shown that the upper limit on gain-bandwidth product should vary inversely as the square of the source of the source-drain spacing. The masking arrangement consists of a fine wire grill of variable wire spacing mounted close to a glass plate, whose lateral position relative to the wires can be adjusted from outside the vacuum enclosure. An additional set of movable masks positioned between the wire grill and the evaporation source serves to define the length of evaporated strips and provide lateral connections for circuits. With this type of jig, it is possible to deposit complete thin-film circuits containing many active and passive elements *in one evacuation*.

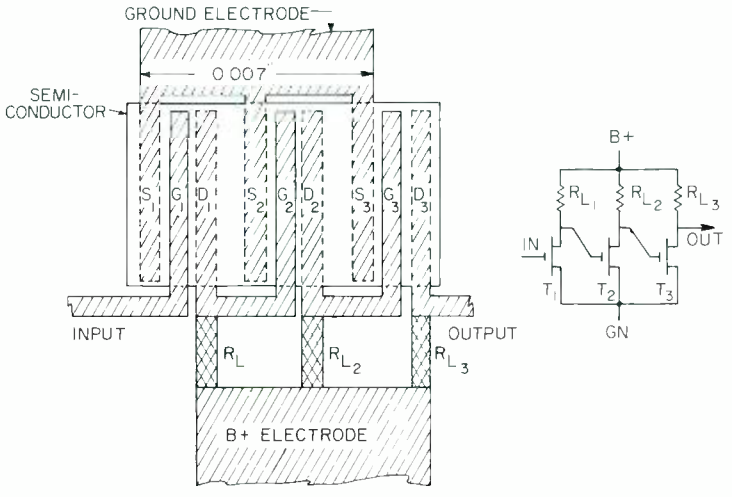
THE TFT IN THIN FILM CIRCUITS

The ability to fabricate circuits and components in the same operation points directly toward the *integrated circuit* concept now being investigated in various forms in several laboratories. [*Editor's Note:* see Kihn, this issue.]

Although in an early stage of development, the TFT thin-film circuit is believed to offer some significant advantages when compared with existing techniques for forming transistors and circuits upon a single-crystal block of silicon. An insulating substrate of nearly unlimited size permits a large array of circuits to be deposited on a single, continuous support. In addition, the electrically inert base offers greater freedom in the design of the active elements and in the geometrical layout of intricate circuit patterns, since active and passive elements can be deposited in layers in any order.

Both of these factors should lead not only to greater circuit density in complex devices, but also to new applica-

Fig. 4—Three-stage direct-coupled thin-film amplifier. Direct coupling is feasible because the insulated-gate TFT does not draw appreciable gate current.



tions where the available space for the electronics is at an absolute minimum. A TFT circuit could, in principle, be deposited upon any part of an existing device offering a few square millimeters of free surface. If the surface is a metal, a preliminary coating of insulator would be applied as substrate for the TFT.

Circuit Fabrication—Three-Stage Direct-Coupled Amplifier

The fabricating of thin-film circuits incorporating transistors, resistors, capacitors, and diodes can be carried out by the same evaporation techniques as for the TFT. To illustrate the method, a three-stage direct-coupled thin-film amplifier was built (Fig. 4). Since many components are deposited simultaneously, the number of operations required for a complete circuit increases very slowly—or not at all—with increasing complexity of the circuit. Complete circuits containing hundreds or thousands of active elements deposited in one evaporation sequence appear to be entirely feasible.

Flip-Flop, AND-Gate, NOR-Gate

Some preliminary consideration has been given to the application of the TFT in miniaturized computer circuits. Although the basic elements of a computer could be constructed using TFT triodes in combination with other thin-film components, it may be advantageous to evaporate multi-electrode active elements designed particularly for the required function.

Fig. 5 illustrates *and* and *nor* gates derived from the TFT. The semiconductor itself is used as the load resistor for the *nor* gate. Fig. 6 shows a direct-coupled flip-flop based upon the TFT. By inverting one of the triodes in the flip-flop, the cross connections are simplified.

The thin-film circuits of Figs. 4, 5, and 6 illustrate only crudely the potentialities of the TFT in integrated-circuit design. It is apparent, however, that the distinction between components and circuits will become more and more diffuse when devices of extreme complexity can be fabricated in one coherent piece. To adequately design, build and use such integrated devices, *a new type of engineering skill will have to be developed.*

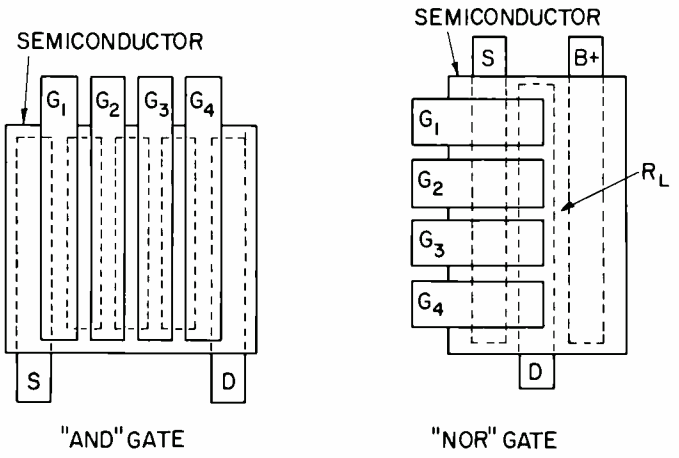


Fig. 5—Thin-film AND and NOR gates derived from the TFT.

CONCLUSIONS

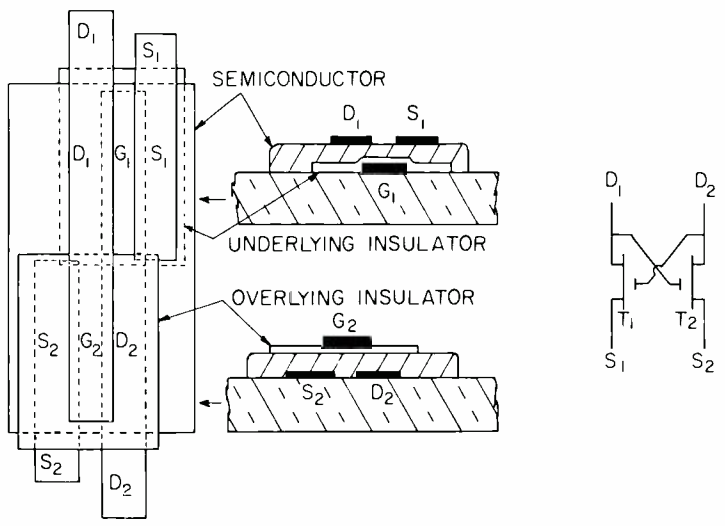
A striking aspect of the TFT development is the demonstration that a high-gain transistor can be built using a semiconductor as imperfect as a polycrystalline evaporated layer. Equally significant is that these transistors operate by the the control of injected majority carriers with an insulated-gate structure. While the close spacing of electrodes has contributed to the surprisingly good performance, the results are a convincing demonstration of the potentialities of devices utilizing injected majority carriers in a wide-bandgap materials. Considering that TFT's have oscillated at frequencies up to 17 Mc using layers of the type yielding Hall mobilities of the order of 5 cm^2/volt-sec, the prospect for improving the frequency response by one or two orders magnitude appears good. This may require materials having higher mobility and structures with closer spacings.

On the basis of the results to date, the TFT appears ready for evaluation in thin-film circuit applications. However, it is clear that much development work remains to be done. Questions such as stability, need for encapsulation, ability to meet design tolerances, etc., have yet to be answered to fully assess the impact the TFT will have on circuit design. If these results are favorable—as preliminary tests appear to indicate—this impact could be very great indeed.

ACKNOWLEDGMENTS

The author expresses his appreciation to Dr. A. Rose and Dr. D. O. North for stimulating discussions, H. Borkan for help in evaluating the performance of the TFT, H. Lambert who performed the precision evaporation on the earliest units, Dr. Frank Shallcross and Dr. J. Dresner for advice on preparation of CdS films, and Dr. H. Johnson for helpful criticism of this paper. Others who have contributed in the fabrication and evaluation of the TFT are V. Frantz, R. Schilling, R. Pugliesi, and W. S. Homa.

Fig. 6—Thin-film flip-flop element equivalent to two TFT's with direct-coupled cross-connections.



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MICROMINIATURE PACKAGING

Implications and Problems

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THE IMPACT of circuit packaging utilizing *microminiature*, or microelectronic, concepts is being increasingly felt in electronic-equipment design. The volume of published literature, abundance of presentations at symposia, and frequent publicity releases all emphasize that the industry is investing huge sums of money on techniques for immediate use, as well as on extensive research programs to develop new concepts for tomorrow. Among the numerous reasons for this trend are three basic factors:

1) *to satisfy military requirements*, where weight and physical size are critical;
2) *to create new markets*, through equipment mobility and portability unattainable with larger-size conventional designs; and
3) *to increase the speed of equipment*, since signal-transit-time requirements can determine to a large extent the physical limitations of hardware.

A relatively few years ago, development of the printed circuit, coupled with useful semiconductor devices, provided real breakthroughs; but, conventional printed circuits involve discrete components lying in the same plane—a two-dimensional character that does not lend itself to maximum miniaturization. Thus, the current tendency is to use the printed board for interconnection of *packaged circuits*, or modules, using efficiently the third dimension.

PACKAGING TODAY—A DIFFICULT PERIOD OF TRANSITION

Important accomplishments in high-density packaging are being achieved in such module development. But it is also in this area where a "numbers" controversy exists—i.e., what component densities can actually be achieved now in a *practical* equipment design? Is the conventional component dead?

In trying to answer such questions, product designers are in a turmoil, caught in a sort of interim trap. The current outpouring of claims and counterclaims make it difficult for the product engineer to judiciously determine what is a statement of *accomplished fact* and what is a projection of *hope for the future*. The more-advanced packaging approaches are not—in reality—at the practical production stage; yet customers, well aware of the microminiature *concepts*, are expecting their immediate use in preference to the "old-fashioned" conventional circuits.

Progressive interim techniques are, therefore, being developed to satisfy current customer demands. Yet, even these require more-sophisticated or at least changed production methods. The obsolescence of existing facilities and the possibility of mushrooming capital expenditures are critical problems facing production activities, in light of the necessity to miniaturize balanced against the ever-changing techniques.

This, then, is the status of the circuit-packaging industry—*a difficult period of transition*. Conventional packaging is looked upon as obsolete, yet really advanced packaging is still in research and development—so interim measures must meet customer demands.

Some questions in this essential, highly active, and sometimes controversial field of packaging are: *What are some of the present problems in applying microminiaturization techniques to products? Where is the present industrial concentration of effort? What is the packaging future?*

Before trying to answer these objectively, it is first helpful to discuss the many microminiature approaches relative to those primary, distinguishing characteristics that are especially significant to the equipment designer.

In Fig. 1, microminiature packaging is classified under the following three main categories:

1) *Discrete component packages*—assemblies of components that are separable, physically or electrically; a one-for-one replacement of conventional components with those of smaller size or uniform form factor, using mountings and connections that contribute further to size reduction. The RCA micromodules[2] and the various minimodules[1] are examples.
2) *Film circuits*—thin films on a substrate to form active and passive components *and* interconnections;[3,4] circuit-oriented, with a one-to-one correlation between components in thin-film and conventional form. The RCA solid-ceramic approach is one form.
3) *Functional blocks*—circuit functions obtained from physical phenomena in an altered semiconductor material; function-oriented, with *no* electrical or physical distinguishability between individual parts. The molecular-electronics approach[3] is an example.

Size and Weight Reduction

Size and weight reduction is achieved by fabrication techniques that either involve the dense packaging of individually miniaturized components, or utilize advanced material processes such as deposition, vapor growth, doping, or diffusion to form inherently small and light-weight components, circuits, or functions.

Reliability

Increased reliability is usually attributed to the reduction of the numbers of solder connections, the replacement of soldered connections with inherently more reliable joints, the reduction in the number of interconnections in general, the utilization of redundancy on the component or circuit level, the structural characteristics of the package, or combinations of each. Unfortunately, microelectronics *does not automatically* lead to higher reliability. Large quantities of meaningful performance data must be accumulated before any credence can be placed in a statement of improved reliability.

From the viewpoint of meaningful performance data, the RCA micromodule is the only presently available microminiaturization program. More experience data has been acquired on RCA's micromodule than on any other microminiaturization program, since it involves the nation's most extensive life-

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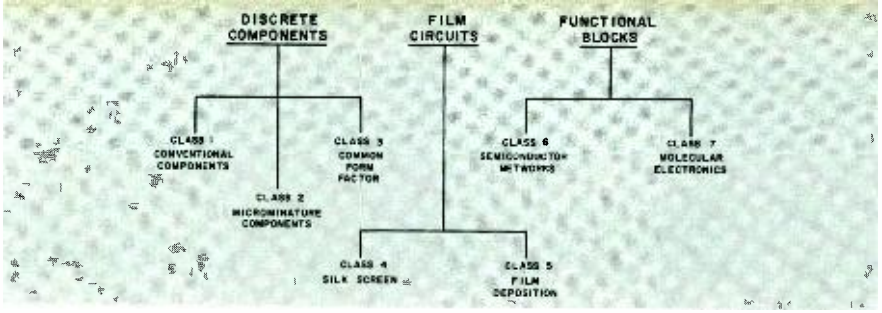


Fig. 1—Microelectronic circuit packaging; the higher the numerical "class," the more dense the packaging capability.

test program for microminiaturized circuitry. As of December 11, 1961, the 412 micromodules placed on Operation Life Test have accumulated 32,022,000 element hours of testing with an estimated mean-time-between-failure of 213,480 hours; the per-module failure rate is 0.47 percent per 1000 hours.

Cost Reduction

Cost reduction in microelectronics is often considered a by-product of improved mechanized construction and assembly techniques, closely allied to yield, volume production, and sales. However, the *true* cost-saving advantage of microminiaturization *is most noticeable at the systems level*—with the big payoff in the reduction of system support costs.[2] Long wiring runs, expensive connectors for entering and leaving cabinets, the cost of cabinets and floor-space requirements are minimized; and, with experience in a particular technique, production-personnel costs can likewise be kept to a minimum.

PRESENT PROBLEMS

Amid the hopes of achieving the ultimate objectives in microelectronics, there remain several fundamental problems that are still evading positive solution. These are 1) *power requirements and heat dissipation*, 2) *microfabrication compatibility or system integration*, 3) *circuit adjustability*, and 4) *the attendant factors related to cost and reliability that were briefly mentioned previously.*

Power and Heat Considerations

Unless effective, positive solutions are found to power and heat problems, the optimum size and weight potentials of microminiaturized systems *will not be realized.*

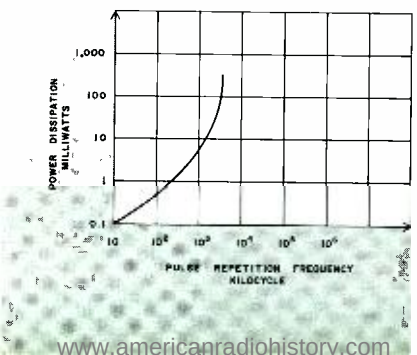
There are several ways in which power dissipation can vary. Circuit power dissipation will increase as the speed of operation increases. For example, energy dissipation can vary as in Fig. 2, the variation of pulse-repetition frequency of a typical transistor flip-flop shown as a function of the power-dissipation level of the circuit. The nonlinearities in the curve result from the nonlinearities of the circuit components and the limitations of the active devices.

Power dissipation in a circuit is likewise a function of resistor and power-supply tolerances. Fig. 3 relates circuit power dissipation and resistor tolerances for different power-supply tolerances. Standby power dissipation refers to the power dissipation of the circuit, not including the power into the load. The dashed *equitolerance locus* illustrates the variation of dissipation with equal resistor and supply-voltage tolerances. If worst-case deviations of 12 percent are assumed for both the resistors and supply voltages, Fig. 3 indicates that the circuit power dissipation is doubled over the dissipation of 100 mw with ideal resistors and supply voltages (zero tolerance).

Figs. 2 and 3 relate the effect of component and operational characteristics on circuit power dissipation. Power-dissipation requirements of a circuit limit the component packing density for allowable temperature difference (Fig. 4). In Fig. 4, a 1-inch cube of germanium, under idealized heat-sinking conditions, is utilized to illustrate the relationship between element power dissipation and packing density (elements per cubic inch). Unfortunately, the packing densities illustrated for idealized thermal conditions *are drastically reduced* for more realistic situations. If each element in a unit volume dissipates 100 mw and the allowable temperature rise in the package is 20°C, a packing density of 7500 elements per cubic inch may be achieved assuming an infinite heat sink on all sides of the cube. Under a more realistic situation, assuming natural convection cooling, the packing density is reduced from 7500 to 4.5 elements per cubic inch.

It is, therefore, obvious that microminiature packaging forces circuit redesign. Extreme reduction in package size is useless unless accompanied by a corresponding reduction in circuit power dissipation.

Fig. 2—Flip-flop pulse-repetition frequency vs. power dissipation.



Microfabrication Compatibility—The Importance of System-Level Packaging Design

Microfabrication compatibility refers to the ability to microminiaturize enough of a given system to realize *on the system level* the size, weight, cost, and reliability advantages.

If the ultimate in miniaturization is to be realized, a *change* in equipment design philosophy is required: The traditional divorce of component, circuit, and system design must yield to a system-oriented marriage philosophy operating within the constraints of the packaged devices, circuits, or functions. At the system-design level, consideration must be given to mounting, interconnecting, and cooling the packaged circuits. If the basic aim in the system or equipment design is directed toward quantitative improvements in size, weight, cost, reliability, and performance, the package must be considered *as a whole.* Cross-over points of optimum design must be established between: 1) interconnection reliability of supporting equipment (back-plane wiring, inter-rack cabling, etc.); 2) support-equipment costs per circuit (module mounting, cooling, etc.) and 3) packaging density in terms of modules per rack.

Consider a portion of this problem—the interconnection of a group of modules on a plug-in printed-wiring card. The designer can choose from two distinct approaches or some design trade-off between these two:

Logic-on-card involves placing the maximum number of interconnections between modules on the board with a minimum of output leads at the connector. Maximum packing density is achieved and back-plane wiring is minimized; *but,* design time is increased and stocking of spares is more of a problem, since a large variety of board types must be used.

With *universal logic,* all input-output signals are brought to the connector. The number of modules on a board is restricted by the pin limitations of the connector: Design time is reduced and the stocking of spares is simplified, since only a few standard units are required per equipment; but, back-plane-wiring is increased, and packing density is usually 30 to 40 percent less than in the logic-on-card technique.

Then, even assuming optimum packaging of the logic circuitry, it must be remembered that in a typical computer logic circuitry accounts for perhaps

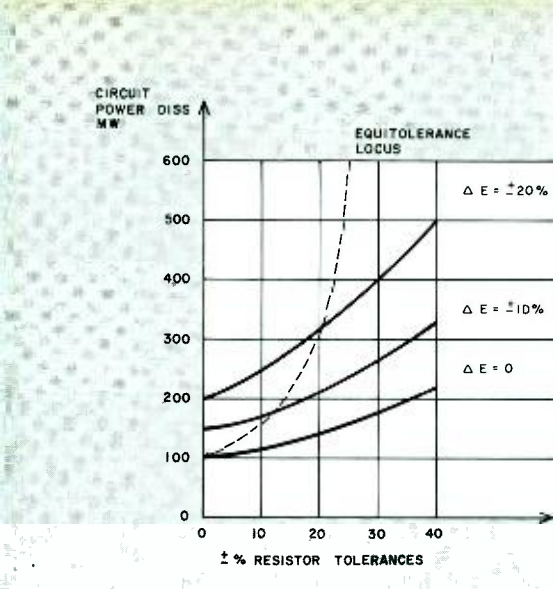


Fig. 3—Standby power vs. resistor tolerances.

only 30 percent of the hardware, while 70 percent may consist of the memory (25 percent), the power supply (30 percent), and the control panel (15 percent). Obviously, such hardware, as well as the logic, must be correspondingly miniaturized if the advantages of the micro-electronic concept are to be fully realized *from a system viewpoint.*

Circuit Adjustability

Too often, the published literature on microelectronic packages ignores the problem concerned with the aligning of complex equipment. This would imply a level of circuit design and stability that is nonexistent. The RCA micromodule, however, is one of the few sophisticated techniques that has provided for circuit adjustability. In the micromodule, the end wafer is provided with a hole through which LC tank circuits and variable capacitors may be adjusted *after encapsulation.* The hole is sealed after adjustment is completed.

Needs in the Thin-Film Approach

In the discrete-component package, the present state of materials knowledge and development is probably adequate to support packaging progress for some time. In the other packaging categories (thin films and functional blocks), a continuing need for materials research exists. In thin-film applications, for example, there remains a requirement for high-dielectric thin films to make possible capacitances of higher value than now attainable, for thin-film inductances higher than the low-microhenry range, and for thin-film active devices.

In general, the thin film packages of today are combinations of thin-film passive components and ultraminiaturized, discrete active components. The capability to produce thin-film active devices is not widespread in the industry. RCA has, however, made a significant breakthrough by developing experimental thin-film cadmium sulfide transistors.[6] This development may well provide the necessary impetus to spur the industry towards the solution of other material problems.

It is generally accepted that the continued research and development in packaging will effect an increasing availability of sophisticated thin-film and functional network packages. Thin-filmed passive circuitry is with us today, and breakthroughs similar to the RCA thin-film transistor are imminent. In some cases, functional networks are in the offering. Certain companies have announced the availability of production quantities of compatible sets of digital semiconductor networks at relatively low costs.

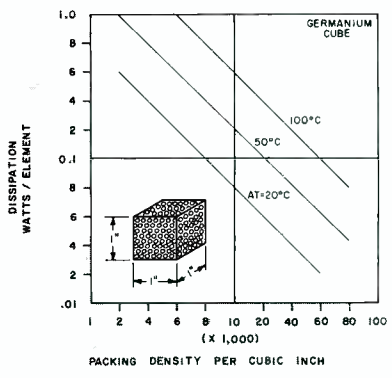
PRESENT INDUSTRIAL UTILIZATION

In spite of rapid advancements in the state-of-the-art of packaging, complete thin-filmed and functional-block circuit packages are not found to any large extent in military equipment.

The EIA P. 9 *Committee on Printed and Modular Components* recently concluded an industrial survey indicating that approximately 85 percent of present-day packaging effort is in the discrete-component area, while close to 90 percent of the effort in this area utilizes conventional components. This current, continuing use of conventional packaging is symptomatic of the lead time necessary before the highly-publicized, more-sophisticated packages can match the present ready availability, general low cost, and proven reliability; simplified testing, stocking, and breadboarding; and flexibility in adaptation of discrete-component packaging. *The conventional component is therefore not dead.*

The EIA survey further indicated that there is extensive development effort on welded modules (discrete-component). The growth of the Welded Packaging Association substantiates this—formed in 1959 with 12 firms, now composed of more than 80 member firms. As a technique for making component connections, welding promises increase in reliability and reduction in size of the welded connection in comparison with the soldered connection. In addition, welding subjects components to a lower in-process thermal stress than does soldering and, thereby, allows connections closer to heat-sensitive devices.

Fig. 4—Dissipation vs. packing density, infinite heat sink.



In summary, discrete-component approaches—minimodule, micromodule, and cordwood techniques—are expected to dominate the scene during the next five years. The advanced techniques—thin films and semiconductor networks—are expected to expand to more prominent positions in 1965-70 (Fig. 5). However, note that the use of conventional components will likewise expand, as the total volume expands at a rapid rate through that period.

CONCLUSIONS

Each of the many packaging techniques has its own optimum area or areas of application, but *no one technique* is universally the best. Consequently, for each intended application, the equipment designer must critically evaluate microminiature feasibility and select the most beneficial techniques from an overall systems viewpoint. At least in the near future, microminiaturized systems will be hybrid structures employing discrete components combined with those thin films and functional blocks that become available—in a practical sense—to the equipment designer.

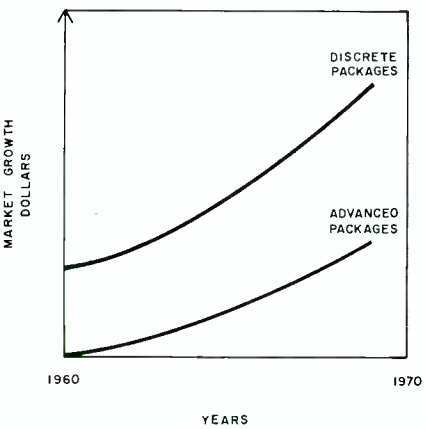


Fig. 5—Packaging market growth prediction.

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SUPERCONDUCTIVE COMPUTER CIRCUITS, ELECTROMAGNETS, AND TUNNEL DEVICES

Current R & D suggests that superconductive phenomena will soon find practical application in such diverse areas as computers, microwave amplifiers, and plasma power generation. This paper reviews briefly the basic aspects of superconductivity and then discusses three applications currently under investigation at DEP Applied Research—superconductive thin-film computer circuits, superconductive electromagnets, and components using electron tunneling between superconductors.

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ANASTAS (TOM) BOORNARD received the BS from the College of William and Mary in 1953 and the MS in Physics from Indiana University in 1955. While at Indiana University, he was a teaching associate in the Physics Department. From 1955 to 1957 he served with the U. S. Army and a member of the Arsenal's Physics and Mathematics Branch, he investigated radiation effects in metals and thin metallic films and performed general studies of the physical properties of metallic films. He came to RCA in 1957 and has been in DEP Applied Research since that time. He has worked on gamma ray and neutron damage in semiconductors, weak magnetic-field detection techniques, and the effects of nuclear-burst-induced ionization on electromagnetic wave propagation. He has also been participating in an Applied Research plasma program, concerned with the conductivity of dense, high-temperature, flowing plasmas produced by a plasma arc jet. For the past three years he has been investigating superconductivity, including the switching characteristics of superconducting alloy films, their application to digital logic devices, and applications of high-critical-field superconductors. Mr. Boornard has been active in the Haddonfield High School Science Senior Program, having served as program chairman during the past term.

SUPERCONDUCTIVITY, characterized by the complete loss of the electrical resistance of some metals at temperatures near absolute zero, was discovered by H. K. Onnes of Leiden University, The Netherlands, in 1911—three years after he attained the necessary low temperature by liquefying helium.[1] Since then, many interesting and potentially useful devices based upon the phenomenon have been proposed. However, until rather recently, even basic research in superconductivity was seriously limited by the expense and delay incurred in constructing apparatus for producing liquid helium.

The development of a reliable, relatively-low-cost helium liquefier in 1946[2] and the imminent availability of lightweight, transportable helium refrigerators[3] have led to an acceleration of research in superconductivity and have stimulated development of devices based on this phenomenon.

Although about half of the metallic elements superconduct, none of the ordinarily good conductors (copper, silver, gold) are superconductors. Some of the more frequently used superconducting elements are presented in Table I, which lists: 1) *critical temperature*, T_c, at which a metal enters the superconducting state in absence of a magnetic field; and 2) *critical magnetic field*, H_{c_0}, that is necessary to drive a metal from the superconductive to the resistive state at 0°K. (Superconductivity has also been observed in 16 other metallic elements and in numerous alloys and compounds.)

Fig. 1—Resistance vs. absolute temperature.

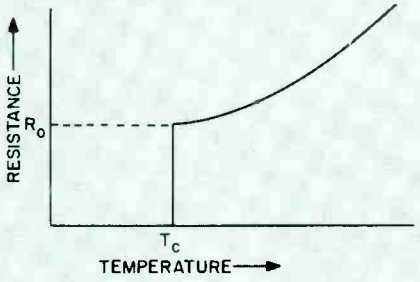
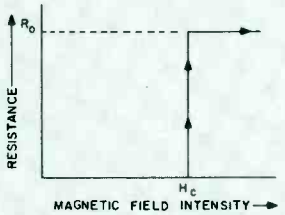


Fig. 2—Resistance vs. magnetic field intensity at temperatures below T_c.



PROPERTIES OF SUPERCONDUCTORS

No experiment has ever succeeded in revealing any trace of DC resistance in a metal when in the superconducting state. The most sensitive experiments are attempts to detect a decrease in a persistent current induced in a superconducting ring. An experiment of this type was performed by Collins[4] with a superconducting lead ring carrying a current of several hundred amperes. There was no observable change in current for a period of about two years.

Superconductors also exhibit the interesting property of magnetic field expulsion — the *Meissner effect* — which cannot be explained merely by zero resistance. If a superconductor was only a zero-resistance metal, a magnetic field could be established within it by first making the metal specimen resistive. If the specimen were then returned to the state of zero resistance, the magnetic field would remain trapped within the specimen because screening currents, which now encounter no resistance, would be set up to oppose the change in magnetic flux. However, for superconductors, the reverse effect occurs — the magnetic flux is expelled from the interior of the metal when it becomes superconducting.

Fig. 3a—Electron distribution vs. energy, normal metal.

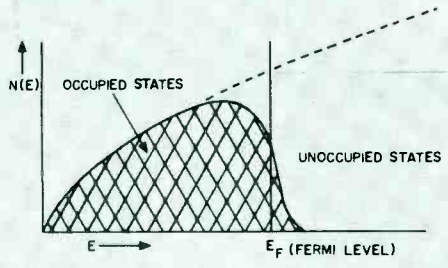
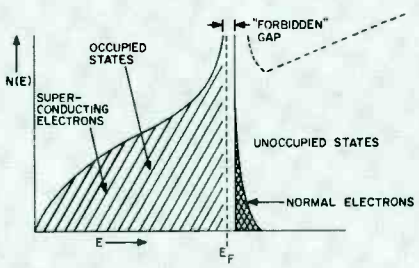
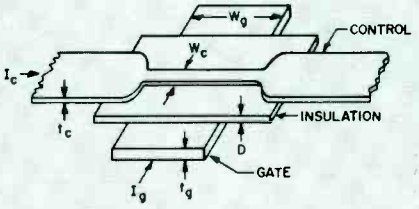


Fig. 3b—Electron distribution vs. energy, superconductor.





JOSEPH P. McEVOY graduated from St. Joseph's College with a BS in Physics in 1959. He expects to receive the MS in Physics this year from the University of Pennsylvania. Since joining RCA, he has been concerned with various solid-state phenomena such as electrostatic printing, electroluminescence, and superconductivity. He has conducted investigations into the characteristics of photoconductive-electroluminescent devices such as high-resolution display media and was instrumental in the development of materials and techniques used in color electrophotography. His experience with the computer field includes work on an electro-optical high-capacity random-access memory and an experimental investigation into the materials and techniques to be used in superconductive digital computer devices. He is presently investigating the tunneling effect between superconductors and the application of other superconductive phenomena to new electronic devices. This past summer, Mr. McEvoy attended a special course on superconductivity given at the Massachusetts Institute of Technology. He is a member of the American Physical Society, Society of Motion Picture and Television Engineers, and Sigma Pi Sigma.

Basic Theory

The complete and abrupt loss of resistance of a superconductor is presumably a consequence of some fundamental change in the electronic structure of the metal. Phenomenological and fundamental theories of superconductivity have been proposed, and both have successfully explained some of the properties of superconductors. A fundamental theory currently gaining wide acceptance is that proposed by Bardeen, Cooper, and Schreiffer.[5] According to this theory, correlated pairs of electrons couple to the lattice vibrations in a nondissipative manner as they traverse the superconductor in a fashion first indicated by Frohlich.[6] The theory also accounts for the Meissner Effect and the dependence of the critical temperature on the isotopic mass.

It follows from this theory that a gap exists in the distribution of the electronic energy levels in a superconductor. The close agreement between recent experimental results on electron tunneling between superconductors and calculations based on a simple model employing this energy gap demonstrate the validity of the Bardeen, Cooper, and Schreiffer theory.

Significant Properties

There are three principal properties of superconductors used in the applications that will be discussed in this article:

1) complete loss of resistance at temperatures below the critical temperature;
2) restoration of resistance by the action of a magnetic field exceeding the critical magnetic field;
3) existence of an energy gap between superconducting and normal electrons and a unique energy distribution about this gap.

The resistance of the metal decreases gradually with decreasing temperature until the metal is cooled to the critical temperature T_c, at which point the resistance drops abruptly to zero (Fig. 1). The lowest resistance attained before the sudden drop is called the residual resistance, R_o. The residual resistance can vary from about 10^{-1} to 10^{-3} of room-temperature resistance depending upon the purity, degree of crystallinity, and if the metal is an alloy, on composition.

The restoration of resistance by the action of a magnetic field is illustrated in Fig. 2. As long as the metal is maintained at a temperature below T_c, the resistance remains at zero despite increases in the magnetic field until the critical magnetic field H_c is attained. At this point, the resistance changes discontinuously from zero to R_o. For ideal superconductors, a parabolic relationship exists between T_c and H_c:

$$H_c = H_{co}\left[1 - \left(\frac{T}{T_c}\right)^2\right] \qquad (1)$$

Where: H_{co} = the critical field at absolute zero.

The distribution of electrons as a function of energy in a normal metal is shown in Fig. 3a. The function $N(E)$ gives the number of electrons per unit volume in the unit energy range between E and $E+dE$. This same function for a superconductor is shown in Fig. 3b according to the Bardeen-Cooper-Schreiffer theory. For the superconductor, there is an excess of occupied states at energy levels below the edge of an *energy gap*, or forbidden region, centered at the Fermi level E_f. Above this gap, there is an excess of available states for electrons. Electrons below the energy gap are in the superconducting state, and those above are in the normal state. The magnitude of this gap is dependent on both temperature and magnetic field. At 0°K and zero magnetic field, the gap width is proportional to kT_c, where k is Boltzman's constant.

SUPERCONDUCTIVE THIN-FILM LOGIC CIRCUITS

The first superconductive logic circuit was demonstrated in 1956 by the late D. A. Buck, whose switching component was a wirewound element called the *cryotron*. A typical wirewound cryotron consists of a 0.009-inch-diameter tantalum wire gate element whose resistance is controlled by the magnetic field of a surrounding single-layer control solenoid of 0.003-inch-diameter niobium wire.

Table I—Critical Temperatures and Critical Magnetic Fields of Some of the Superconducting Elements

Element	*Critical Temperature T_c (°K)*	*Critical Field, H_{co} (oersted)*
Aluminum	1.18	106
Indium	3.37	269
Tin	3.73	310
Mercury	4.15	413
Tantalum	4.38	860
Lead	7.22	800
Niobium	8.0	2600

Fig. 4—Thin-film cryotron.

Gate mat'l: tin, indium, lead-indium, tin-indium
Gate thickness; t_g: 2000—4000 angstroms
Gate width; w_g: 0.005—0.012 inch
Insulation mat'l: silicon monoxide
Insulation thickness, d: 3000—5000 angstroms
Control mat'l: lead
Control thickness, t_c: 3000 — 5000 angstroms
Control width, w_c: 0.002—0.005 inch

Fig. 5—Cross-section of cryotron circuit films.

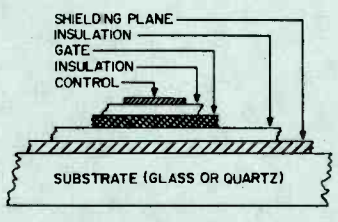
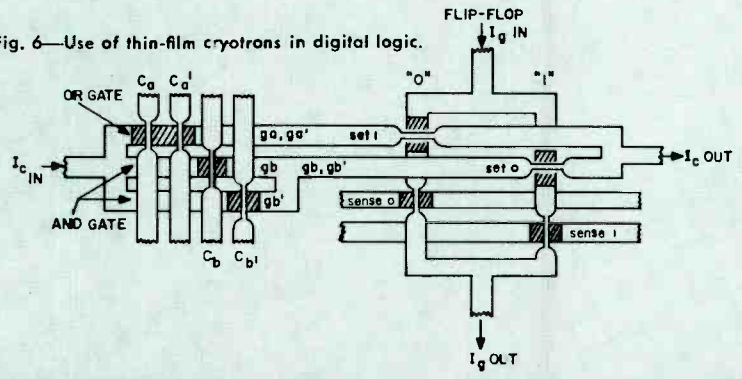


Fig. 6—Use of thin-film cryotrons in digital logic.



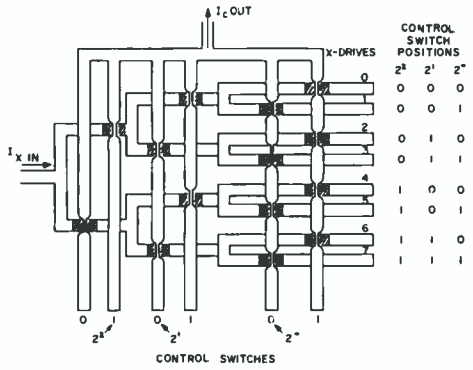


Fig. 7—A thin-film-cryotron fractional-current-gain circuit—the tree multiposition switch.

Thin-Film Cryotrons—An Integrated-Circuit Approach

The early cryotron switching device was slow and somewhat difficult to fabricate, but its counterpart, the *thin-film cryotron*, has nanosecond switching-speed capabilities and is easily batch fabricated by vacuum deposition—a true integrated-circuit approach to superconductive thin-film logic circuits, since complete circuits and their interconnection leads can be deposited on a single substrate by a series of evaporations. While a number of problems remain to be solved before mass production of uniform units is possible, thin-film cryotron circuits, combined with superconductive thin-film memories, offer a promising approach to the development of low-cost, fast, reliable, high-capacity computers. From a system standpoint, the chief problem associated with superconductive computers is the requirement for a low-temperature environment. It is expected that the refrigeration problem will soon be overcome by the perfection of closed-cycle helium refrigerators.

Preliminary efforts to incorporate superconductive thin-film devices into complex computing circuits have uncovered problems in the uniform reproduction of the switching characteristics of thin-film cryotrons. Some success has been achieved through the development of evaporation techniques employing stringent control of the vacuum deposition variables. Further improvements in uniformity will be derived from an understanding of the fundamental behavior of superconductors, especially when in the thin-film form.

The basic thin-film superconductive switching component, usually called the *crossed-film cryotron* (CFC), is illustrated in Fig. 4, along with typical materials and dimensions.

The resistance of the gate film is controlled by the magnetic field associated with the control current I_c. This field causes a small resistive channel to be formed in the gate film, but only under the narrow portion of the control element. Since the control element is made of lead, which has a much higher critical temperature and critical magnetic field than the gate materials, it remains superconducting throughout the entire switching operation.

Circuit Gain

The magnetic field H (in oersteds) acting on the gate element due to the control current I_c (amperes) is:

$$H = 0.2\pi \frac{I_c}{w_c} \qquad (2)$$

Where: w_c is the width (centimeters), and H in Eq. 2 is the horizontal component of the field. (For a flat strip conductor with a large width-to-thickness ratio, the vertical magnetic field component falls off rapidly with distance and can be neglected.) Since the magnetic field acting on the gate is inversely proportional to the control element width, the control element is made narrow over the gate element so that the gate current I_g can be controlled with a control current smaller than I_g. The ratio I_g/I_c is called the current gain.

Current gains of greater than unity are necessary if the output current of one circuit is to be used to drive additional circuits. By adjusting the gate-to-control width ratio, a range of current gains can be realized.

Switching Time

The switching time, τ, of a thin-film cryotron digital logic circuit is directly proportional to the self-inductance of the over-all circuit L and inversely proportional to the cryotron gate resistance R:

$$\tau = \frac{L}{R} \qquad (3)$$

Since the circuit self-inductance is usually many times that of the individual cryotron elements, individual cryotron switching speeds have little meaning.

To minimize τ, L is made as small as possible and R is made as large as possible. By using an alloy as the gate film material, R can be made quite large because the resistivity of alloys is considerably greater than that of single-element metals at low temperatures. Thin-film switching devices using lead-50–indium alloy films as gate materials have been fabricated and operated at 4.2°K at DEP Applied Research. Calculations indicate that for a given circuit, this alloy reduces τ by a factor of 100 over that obtainable with tin, a common gate material.

The circuit self-inductance L can be decreased by using a superconducting shielding plane. This plane is fabricated by depositing a lead film about 4000 angstroms thick on the glass or quartz substrate. This is followed by the deposition of a silicon monoxide insulating film. The deposition of the gate, silicon monoxide, and control films (Fig. 4) then follows. A cross-sectional view of all of the cryotron circuit films is shown in Fig. 5. The circuit self-inductance is reduced when a shielding plane is used because screening currents are set up on the surface of the plane which add to the magnetic field between the plane and the films above it, but which cancel the field everywhere else. The net effect is to reduce the number of flux linkage lines around a current-carrying film and this reduces the film's self-inductance. When a shielding plane is used, the self-inductance per unit length (henrys/cm) of a thin-film located above it is:

$$\frac{L}{l} = 4\pi \frac{d}{w} \times 10^{-8} \qquad (4)$$

Where: w is the film width and d is the thickness of the silicon monoxide film separating the circuit film and the shielding plane.

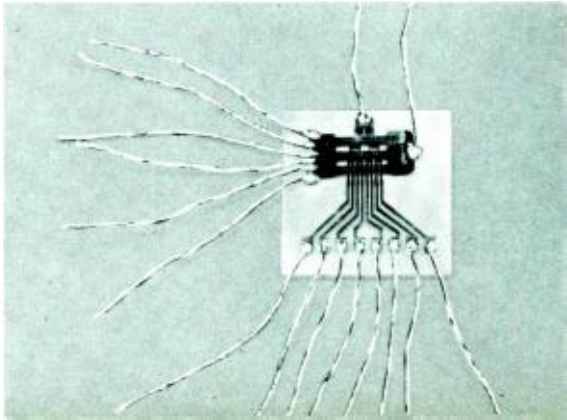
Circuit Design—Or-Gate, And-Gate, Flip-Flop

To avoid excessive dissipation of liquid helium, thin-film cryotrons should be operated as current-driven, current-output devices, thereby eliminating resistors. Further, the cryotron circuits should be designed so that an alternative superconducting path is always available for the circuit current.

The use of thin-film cryotrons in digital logic circuits is illustrated in Fig. 6 by a flip-flop whose *0* state is set by an *or* gate and whose *1* state is set by an *and* gate. The shaded portions in the figure represent a low critical field gate film material.

Control elements C_a and $C_{a'}$ and gate film g_a, $g_{a'}$ perform an *or* function. If a current pulse is sent through element C_a or $C_{a'}$, resistance is introduced into film g_a, $g_{a'}$ and current I_c will flow through branches g_b and $g_{b'}$.

Fig. 8 — Developmental 8-position address switch using 14 cryotrons that occupy an area of 1/16 square inch.



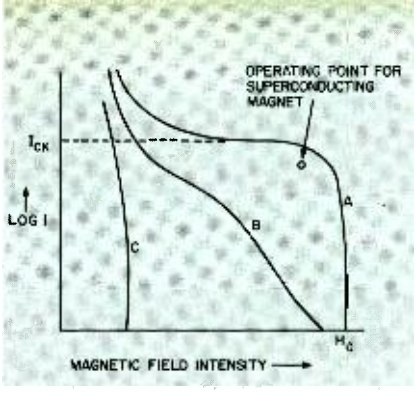


Fig. 9—Effect of mechanical strain on superconductor critical field and current characteristics. A: typical hard superconductor with extreme mechanical deformation. B: partially worked superconductor alloy. C: effect of annealing.

Control elements C_b and $C_{b'}$ and films g_b and $g_{b'}$ perform an *and* function. Current pulses must be transmitted through C_b and $C_{b'}$ to cause I_c to flow into film g_a, $g_{a'}$.

The flip-flop consists of the superconducting thin-film loop containing branches *0* and *1*. The current I_g can be directed through either of the branches. Film g_a, $g_{a'}$ of the *or* gate is made of lead and narrowed over the *0* branch of the flip-flop so that it acts as a control element for this branch. This control, labelled *set 1*, places the flip-flop in the *1* state. Film g_b, $g_{b'}$ of the *and* gate serves as a control element for the *1* branch and places the flip-flop in the *0* state.

The films labeled *sense 0* and *sense 1* can be used to sense the state of the flip-flop or to drive other circuits.

The flip-flop operates as follows: If current I_g is flowing in the *0* branch and the *set 1* control is pulsed, resistance is developed in the *0* branch and I_g is diverted into the superconducting *1* branch. Upon removal of the control pulse, I_g will continue to flow only through the *1* branch of the flip-flop, although the *1* and *0* branches are both superconducting, because magnetic fields would be induced to oppose redistribution. This feature affords great flexibility and simplification in the design of superconductive thin-film logic circuits.

As illustrated in Figs. 4 and 6, the circuit films are made narrow over the gate film regions at which cryotron action is desired and are wide everywhere else. This reduces the self-inductance of a thin-film cryotron circuit loop (see Eq. 4) and thereby decreases the circuit switching time.

Calculations indicate that the circuit switching time τ of a thin-film cryotron flip-flop loop of the type illustrated in Fig. 6 will be about 0.5 nsec, assuming the gate material is lead-50–indium and the current gain is unity.

If the *sense* gates are to drive additional logic circuits, current gain is required. Because the current gain is directly proportional to the ratio of gate width to control width, the circuit can readily be designed to provide the necessary gain. However, the circuit switching time is directly proportional to the square of the current gain. For that reason, switching speed is more severely affected by gain increases than in conventional circuits.

Fractional-Current-Gain Circuits

Thin-film cryotron circuits in which only fractional current gains are required are faster switching and require less critical control of film width and thickness than circuits requiring greater-than-unity gains. Fig. 7 illustrates an example of such a circuit, the *tree multiposition switch*, one type of decoder being developed for addressing superconductive memory planes. (Superconductive memory planes in the form of continuous sheets have been developed by L. L. Burns and his group at the RCA Laboratories, Princeton, N.J.)[7] The integration of superconductive address switches with memory planes is the first step toward the development of an all-superconductive computer.

In Fig. 7, current I_c can be diverted into any of the eight *X*-drive lines depending upon the settings of the three control switches. For example, if *X*-drive No. 4 is to be selected, the 2^2 control switch is set to *1* and the 2^1 and 2^0 control switches are set to *0*.

The tree switch contains 14 thin-film cryotrons. The number of cryotrons N_c required in a tree switch having N_o outputs is:

$$N_c = \sum_{1}^{n} 2^n \qquad (5)$$

Where: $n = \log_2 N_o$. For a *ladder switch* of eight outputs, the number of cryotrons required is $N_c = n2^n$. A ladder multiposition switch of eight outputs would therefore require 24 cryotrons.

A photograph of a developmental eight-position address switch (with wire leads attached for purposes of testing) is shown in Fig. 8. The eight lines that fan out to the right of the switch were intended to lead to eight drive lines of a rather-large, developmental 8-by-8 superconductive memory matrix. More recent memory planes are so much smaller that it is unnecessary to draw out the lines to accommodate the memory drives. The gate films in this switch are made of lead-50–indium; the control films are made of lead.

Table II—Approximate Knee Critical Currents and Critical Magnetic Fields of Typical Hard Superconductors at 4.2°K

Material and T_c*	I_{ck} *(Amperes)***	H_c *(Kilogauss)*
Molybdenum—25–Rhenium	2.0	13
Niobium—33–Zirconium (11°K)	15	70
Niobium—Tin (Nb_3Sn), (18°K)	13.5	>100

* Composition is given in atomic-percent.
** For wires of 0.010 inch nominal O.D.

The 14 cryotrons occupy an area of about 1/16 square inch. This is equivalent to 224 cryotrons per square inch. A stack of 10-mil-thick glass substrates, each containing 224 cryotrons with 10-mil separations between them, gives a component density of 11,200 cryotrons per cubic inch. As more-accurate mask-making techniques are developed, greater component densities will be obtained.

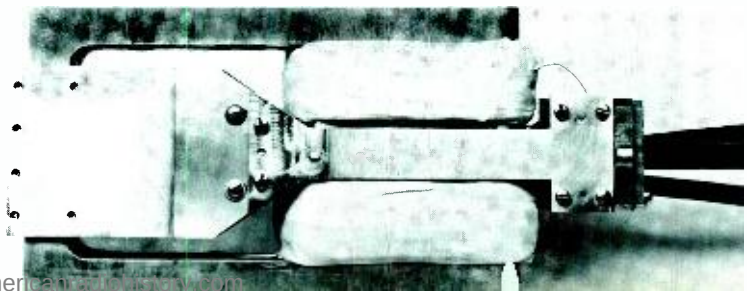
SUPERCONDUCTING ELECTROMAGNETS

The property of zero resistance permits operation of electromagnets without the dissipation of power through Joule heating in the magnet coils. Onnes, in fact, attempted to make a superconducting magnet shortly after he discovered superconductivity. He and others soon realized, however, that superconductivity and high magnetic fields are, in general, incompatible; that is, resistance is restored in a superconductor by a magnetic field of sufficient intensity. The misconception that all superconductors would have relatively low critical magnetic fields dissipated early enthusiasm for superconducting magnets. Recent progress in materials research has shown that this is not true for *hard*, or non-ideal, superconductors. Interest in such magnets has been revived.

Hard Superconductors and Breakthroughs in Electromagnets

One of the significant recent revelations in regard to hard superconductors is that their critical field and critical current characteristics are improved *by increasing the degree of mechanical strain in the material* (Fig. 9).

Fig. 10—Superconductive electromagnet, developed at DEP Applied Research, that weighs 5 pounds, occupies 16 cubic inches, and produces 6 kilogauss.



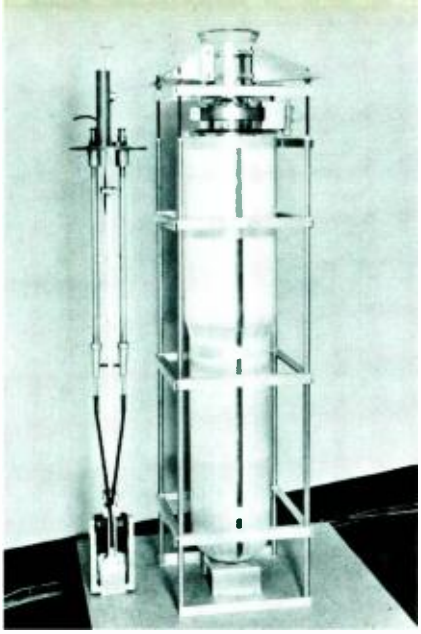


Fig. 11—Magnet of Fig. 10 attached to C-band meander-line maser structure (left), and the liquid-helium dewar equipment used for testing the assembly.

The strained samples (Fig. 9) seem to have a common critical field H_c at very small current values. The levelling off of the critical current with magnetic field is characteristic of samples which have been excessively cold-worked. The value of the current at the knee of the curve is I_{ck}. The quantities H_c and I_{ck} for a wire of given diameter determine the relative merit of the material for superconducting magnet coils. Table II shows approximate values of H_c and I_{ck} for some important high-field superconductors.

A chemical-transport technique for the continuous growth of crystalline niobium-tin which has the highest known critical temperature, 18°K, and a critical field greater than 100 kilogauss has been developed at the RCA Laboratories. By coating a ductile base wire with these Nb_3Sn crystals, thousands of feet of niobium-tin wire can be produced for use in magnet fabrication.

It seems reasonable that superconducting solenoids generating fields of 100 kilogauss or better will soon be practical laboratory devices. In addition to their usefulness in basic research, such high-power magnets may soon be used in magnetohydrodynamic energy-conversion schemes and for magnetic confinement of thermonuclear plasmas. Heretofore, fields of this magnitude could be obtained only by pulsed operation or by expending megawatts of power (as in Bitter magnets).

A Superconducting Electromagnet for Maser Systems

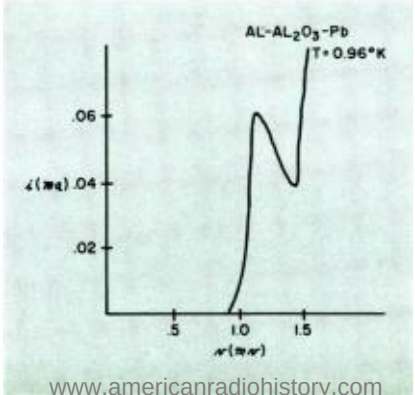
Co-workers in Applied Research have pointed out[9] the need for compact, lightweight, and adjustable magnets to provide the Zeeman splitting of the energy levels in solid-state maser crystals. Since the maser operates in a liquid helium environment, the superconducting electromagnet is in many ways ideal for this application.

A superconducting electromagnet for a traveling-wave maser has been developed at DEP Applied Research and is believed to be the first development of this type, although superconducting electromagnets have been used previously with cavity masers.[10]

In the usual arrangement of a solid-state maser, the maser structure is contained in a set of dewars (vacuum flasks) placed between the pole faces of a conventional electromagnet. Because of the large magnetic gap that results, a conventional magnet which is quite massive and consumes considerable power is required to provide the necessary field uniformity and intensity across the maser crystal. By winding superconducting wire on an iron core with a gap in it, an electromagnet can be fabricated which fits inside the liquid helium dewar. The magnet coils consume no power and only a minute amount of power is dissipated in the copper leads to the coils. The maser with a superconducting magnet provides two significant advantages over a conventional maser system: 1) decrease in size and weight of the maser system, and 2) decrease in system cost and complexity due to negligible power consumption.

The electromagnet developed at Applied Research (Fig. 10) consists of an iron yoke wound with 3226 turns of 0.005-inch-diameter molybdenum-rhenium alloy of 50:50 weight composition. It is designed to produce a magnetic flux density of 6 kilogauss, uniform to within 0.1 percent of its axial value over an active crystal area of 0.35 square inch. The magnet including coils weighs approximately 5 pounds and occupies a volume of about 16 cubic inches. Fig. 11 shows the superconducting electromagnet attached to a C-band meander-line maser structure and the liquid-helium dewar arrangement used for testing the maser-magnet structure. No attempt has been made to minimize the space and weight requirements, since the magnet was designed to fit directly onto an existing maser structure. The high gain-per-unit-length of the meander-line maser indicates that concurrent design on the magnet and the maser would produce a considerably smaller package.

Fig. 12—Current-voltage relationship of a typical superconducting tunneling sandwich, the tunneltron.



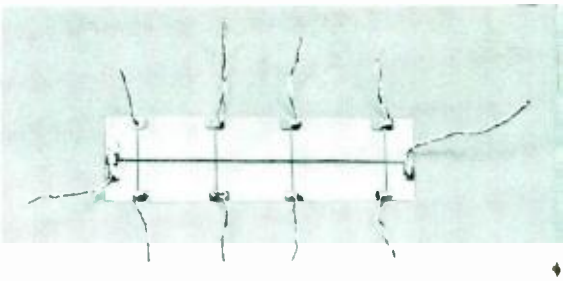


Fig. 13—A superconductive tunnel device, the tunneltron.

The magnet has been tested at 4.2°K and 1.7°K by observing the paramagnetic absorption of a single crystal of chromium-doped titanium (rutile) over the frequency range of 3.85 to 8.66 Gc. Magnetic fields in the range of 3 kilogauss were obtained at currents of about 1 ampere. The highest field obtained is estimated to be 6 kilogauss. Approximately 4.5 liters of liquid helium were required to cool the magnet and maser from 77.6°K (liquid-nitrogen temperature) to 4.2°K after which the helium dissipation rate was about 0.2 liter/hr.

Electron Tunneling Between Superconductors

The knowledge that particles can tunnel through energy barriers is almost as old as the study of quantum mechanics. The misconception that it is a new discovery is due to the recent success of the tunnel diode, which did much to spread appreciation of this subtle phenomenon.

However, electron tunneling between superconductors differs from that in the Esaki model,[11] since the tunneling takes place through a thin dielectric rather than through the charge-depletion region of the semiconductor junction. The barrier that the electron sees after leaving the metal is essentially the energy gap between the valence and conduction bands of the insulator. At very low voltages, the electron never enters the conduction band of the insulator but tunnels directly into the acceptor metal.

The following discussion explains some of the effects associated with tunneling between two superconducting metals, between a superconducting and normal metal, and between two normal metals. The superconducting model employed here is an individual particle approximation (Sommerfeld-Bloch, 1928) with the electronic density of states and the energy gap centered at the Fermi

level consistent with the Bardeen-Copper-Schreiffer theory (Fig. 3).

Transmission Coefficient

The transmission coefficient, or probability of a particle tunneling through a potential barrier, depends exponentially upon the product of the barrier thickness and the square root of the barrier height.

If two normal metal films are separated by an extremely thin dielectric film (barrier), the transmission coefficient for electrons will be large enough for some tunneling current to be observed. Typical insulating layers in tunneling experiments are oxide films in the 20- to 50-angstrom thickness range. For a sandwich of normal metals, the tunneling current will be directly proportional to the applied voltage if this voltage does not exceed a few millivolts.

If the acceptor side of the metal-dielectric-metal sandwich is superconductor, the current-voltage relationship becomes nonlinear. This effect is based on the simple assumption that the tunneling current is proportional to the density of states. Conduction electrons from the normal metal which are at energy levels corresponding to energy values within the superconductor's forbidden region are not accepted by the superconductor and are, in effect, reflected. Only when the energy of the conduction electrons is increased, by increasing the applied voltage, to correspond to the energy states available within the acceptor superconductor can tunneling take place. It is for this reason that no significant tunneling current develops from the application of a low voltage. As shown in Fig. 3, the electrons find the greatest number of available states just above the forbidden region.

Negative Resistance

From an application standpoint, the most important characteristic observed in tunneling is that which takes place when both metals are in the superconducting state but have different critical temperatures. In this case, the current will increase, decrease, and increase again as a continually increasing voltage is applied. The initial increase develops as the voltage raises more and more electrons in the donor superconductor above the forbidden region of the acceptor superconductor. At a certain voltage level, all the normal electrons in the donor superconductor can tunnel into the acceptor. As the voltage is increased beyond this point, the tunnel current decreases because there are fewer available energy states in the acceptor metal. This is the *negative-resistance region.*

Finally, further increases in the applied voltage raises the energy of the electrons below the forbidden region in the donor superconductor to an energy above the forbidden region of the acceptor superconductor and the current increases rapidly because: 1) the number of donor electrons now available is large, and 2) the number of available states in the acceptor is largest just above the acceptor's forbidden region. The current-voltage relationship of a typical superconducting tunneling sandwich (Al-Al_2O_3-Pb) is shown in Fig. 12. This sandwich is commonly referred to as a *tunneltron.*

Applications

Tunnel devices such as shown in Fig. 13 appear to have a large number of applications. For example, when both metals are superconducting, the tunneltron can serve as a negative-resistance diode. When neither metal is superconducting, the sandwich can be used as a resistor or capacitor. When one metal is normal and the other superconducting, the sandwich can duplicate the functions of a diode. By adding external control elements, the characteristics of a triode can be obtained. As in the case of the thin-film cryotron circuits, these sandwich components can be batch-fabricated by the vacuum deposition process.

In DEP Applied Research, initial attempts to fabricate these sandwiches have pointed out some serious difficulties. The device will not produce a useful current level unless the oxide insulation is very thin. Initial experiments have been made with aluminum films oxidized for a few minutes at room temperature. This method is adequate for experimental purposes; however, because the oxide layer thickness is extremely difficult to control, more-precise techniques are being developed.[12]

The usefulness of these tunneling devices in practical circuits will depend upon the extent to which their operating current and voltage levels can be raised. This may be done in two ways:

1) Perfection of techniques for producing extremely thin, uniform dielectric layers that will increase the transmission coefficient and, consequently, the tunneling current.
2) Development of techniques for using higher critical temperature materials (larger energy gap superconductors) to increase the operating voltage of these components.

In spite of some formidable limitations, these devices are versatile, extremely small ($10^{-6}cm^3$), consume minute quantities of power (10^{-9} watts per device), and after certain production problems are solved, will be easy to fabricate in large quantities.

CONCLUSIONS

Reliable low-temperature apparatus has brought about extensive research and development in superconductivity. This phenomenon has yielded fundamental information on electron transport processes in solids, metallurgy, and electron-lattice interactions. In addition to interest for fundamental research, superconductivity offers many possibilities for unique electronic devices. Future computers with billions of elements fabricated by the vacuum deposition of super-conductive logic and memory devices seem feasible. An all-cryoelectric computer may be the next major breakthrough in computing systems technology.

Also, many future communication schemes requiring high magnetic fields such as in masers, etc. may now be considered in a new perspective. Solenoids made from superconducting alloys and compounds will provide the high magnetic fields needed for future research in solid-state physics as well as for magnetic containment of plasmas in thermonuclear and magnetohydrodynamic power conversion systems.

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The David Sarnoff O

The 1962 Individual Awards for Science and Engineering

R. D. Kell

R. D. KELL, a Fellow of the Technical Staff, RCA Laboratories, Princeton, N.J., is recipient of the 1962 David Sarnoff Outstanding Achievement Award in Science . . . *"for many outstanding contributions which continue to lead to major innovations in the field of television."*

MR. KELL, as early at 1926-27, while doing graduate work, implemented a complete operating television system. Then, joining RCA in 1930, he directed development of components for the present television system, including the first high-power, high-frequency television transmitter, the first Iconoscope camera, and the first remote-pickup and radio-relay facility. After W.W. II, his continuing television work included image-orthicon cameras and improved transmission techniques, important contributions to the rapid commercialization of television. In the early 1950's, he contributed significantly to the establishment of compatible color television as a complete working system. He continues to challenge television frontiers: His more recent contributions have been in color videotape recording and color-television reproducers.

R. Lieber

R. LIEBER, Systems Engineering, Moorestown Missile and Surface Radar Division, Defense Electronic Products, Moorestown, N.J., is recipient of the 1962 David Sarnoff Outstanding Achievement Award in Engineering . . . *"for contributions to the field of high-precision space tracking and navigational systems."*

MR. LIEBER has contributed new and fundamental knowledge to high-accuracy prediction of satellite and missile position using surface-based tracking data, which opens new avenues to the solution of satellite tracking problems. He has made important advances in the integration of tracking, communication, and telemetry functions for support of space missions and has also pointed the way toward vehicle attitude determination from the earth. The applications for which he has developed solutions include ship, submarine, and aircraft navigation, and surveying of land locations. He has worked out commercial as well as military systems applications. As an Engineering Leader, he has demonstrated outstanding ability to plan the effort of and obtain maximum wholehearted support from the senior engineering personnel in his group.

The 1962 Tea

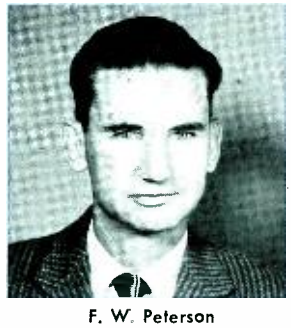
G. B. Herzog

B

J. C. Miller

C

M. Berg



F. W. Peterson

utstanding Achievement Awards

n Awards for Science and Engineering


. J. Lechner


M. H. Lewin


H. S. Miiller


. W. Mueller


H. Nelson


H. S. Sommers

G. B. Herzog, B. J. Lechner, M. H. Lewin, H. S. Miiller, J. C. Miller, C. W. Mueller, H. Nelson, and H. S. Sommers, of the RCA Laboratories, Princeton, N.J., are recipients of the 1962 David Sarnoff Outstanding Team Award in Science . . . *"for team performance in conceiving and developing devices, circuits, and memories for kilomegacycle computers."*

Messrs. Herzog, Lechner, Lewin, Miiller, Miller, Mueller, Nelson and Sommers were members of a project team that undertook basic and exploratory research which has produced advances of great significance in high-speed (kilomegacycle) computers. Their work involved, among other things, a fundamental examination of phenomena and devices capable of extreme data-processing speeds. An important result of this work is basic knowledge about and circuit implementation of the tunnel diode; realization of tunnel-diode logic required the invention of entirely new concepts. The implications of this work for RCA's electronic-data-processing efforts in the future are considerable, for in addition to its significance on this project, their effort has produced a solid technological base upon which computers far beyond the present art can be built. Their work also has led to important basic knowledge and experience that may provide new commercial opportunities for tunnel and varactor diodes.


F. G. Block


M. B. Shrader

M. Berg, F. G. Block, F. W. Peterson, and M. B. Shrader, members of the Cermolox Power Tube Group, Electron Tube Division, Lancaster, Pa., are recipients of the 1962 David Sarnoff Outstanding Team Award in Engineering . . . *"for entirely new concepts in power tube construction which have resulted in compact, rugged, and more powerful ultra-high-frequency tubes."*

Messrs. Berg, Block, Peterson, and Shrader were members of an engineering team that developed a new line of power tetrodes using ceramic envelopes and an internal construction permitting higher power dissipation, higher efficiency, and great ruggedness and compactness for space-age applications. The group achieved two important breakthroughs. The first was ceramic-to-metal seals of great strength which could be manufactured with ease and uniformity. This resulted in the desired compact and rugged external construction. The second was the conception and development of a revolutionary new method of making grids of precise alignment from materials with very high thermal conductivity, which gives the desired high efficiency at UHF and permits higher power output.

. . . About the Awards

RCA has chosen for its highest technical honors, the four *David Sarnoff Outstanding Achievement Awards* for 1962, a scientist, an engineer, a research team of eight scientists, and an engineering team of four engineers. The awards, to be formally announced by Dr. Elmer W. Engstrom, President of RCA, consist of a gold medal, a bronze replica citation, and a cash prize for each man.

The David Sarnoff Outstanding Achievement Awards for individual accomplishment in science and in engineering were established in 1956 to commemorate the fiftieth anniversary in radio, television, and electronics of Brigadier General David Sarnoff, RCA Chairman of the Board. These have been made annually since then to one scientist and one engineer.

The two awards for team performance were initiated in 1961.

All engineering activities of RCA divisions and subsidiary companies are eligible for the Engineering Awards. The Chief Engineers in each location may present nominations annually. Similarly, members of the research staff of the RCA Laboratories are eligible for the Science Awards. Nominations are made by the Research Directors.

The selection committee for both the individual and team awards in engineering includes: the Vice President, Research and Engineering, Chairman; the Staff Vice President, Product Engineering; the Director, Communications Engineering; the Vice President, RCA Laboratories; and the Vice President, Personnel.

The selection committee for both the individual and team awards in science consists of: the Vice President, Research and Engineering, Chairman; the Staff Vice President, Product Engineering; the Vice President, RCA Laboratories; the Associate Director, RCA Laboratories; and the Vice President, Personnel.

EPITAXIAL DOUBLE-DIFFUSED SILICON SWITCHING TRANSISTORS

Epitaxial technology allows deposit of single-crystal films of high resistivity on single-crystal substrates of very low resistivity. Application of this new technique to diffused-base and diffused-emitter silicon transistors provides characteristics which are superior to those of non-epitaxial prototypes. Described here are design concepts and basic processing steps of the 2N1708 silicon transistor, an epitaxial version of the 2N708.

Dr. A. BLICHER, Mgr. *GaAs Product Devel.*
H. KRESSEL, Ldr. *Microwave Diodes*
Dr. H. S. VELORIC, Mgr. *Si Computer Products*

Semiconductor and Materials Division, Somerville, N. J.

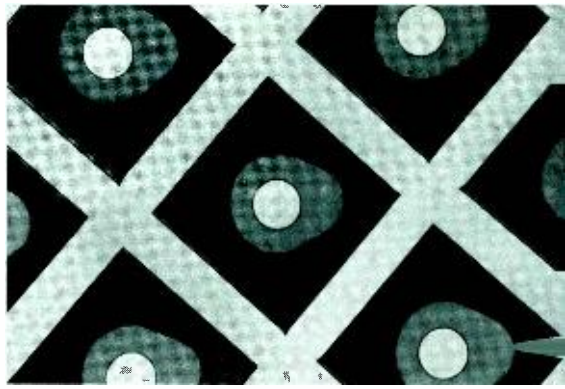


Fig. 3a—Array of diffused base areas defined in SiO_2 (abt. 400x).

THE 2N1708 silicon transistor illustrates the concepts of planar epitaxial design. The dimensions and process specifications given in Fig. 1 and Table I were selected on the basis of current-handling requirements, other pertinent electrical characteristics, and the ability to control the many processing operations.

Fig. 2 shows the processing steps used in fabricating the 2N1708. To ensure quality control, production personnel check fabrication steps by microscope examination, such as shown in Figs. 3a-3d, a necessity in order to detect any minute imperfections that might affect device performance.

The lightly doped collector is grown on the heavily doped substrate by use of epitaxial techniques. A layer of silicon dioxide is thermally grown on the silicon wafer. The collector area is then defined in the oxide by means of photolithographic and acid-etching techniques. The p-type base layer is introduced by depositing and diffusing boron. The emitter area is then defined on the base area, and a heavily doped phosphorus layer is diffused until a base width of less than one micron is achieved. Fig. 4 shows the net impurity distribution achieved by this process. After an additional oxidation step, the region to be metalized is etched away and aluminum contacts are evaporated and alloyed.

QUALITATIVE DESIGN CONCEPTS

It is beyond the scope of this paper to evaluate the parameters[1,2] of a transistor in detail. This section will indicate only what effect the device geometry and fabrication process have on device characteristics.

Table II compares the important electrical characteristics of a non-epitaxial double-diffused transistor, the 2N708, with its epitaxial counterpart, the 2N1708. Table II also shows the significant design parameters which influence each characteristic. Some of these interrelationships are discussed below.

The *junction breakdown voltage*, V_{cbo}, is principally determined by the doping level of the collector region, $|N_D-N_A|$. In an epitaxial device, it is possible to decrease the impurity concentration, and thus increase V_{cbo}, without degrading other characteristics.

For a given circuit and transistor current gain and at moderate current densities, the *saturation collector-to-emitter voltage*, $V_{ce}(sat)$, is primarily determined by the collector spreading resistance, R_{sc}. Because the high-resistance region is only a few microns thick in an epitaxial structure, the resistance is reduced from 50 ohms for the 2N708 to a few ohms for the 2N1708.

The *base-to-emitter voltage*, V_{be}, is determined by the sum of two terms which for a given semiconductor device depend on the geometry, impurity levels, and current levels. The base spreading resistance, R_b', is mainly determined by the base sheet resistivity and the base contact geometry.

The *collector junction capacitance*, C_c, is determined by the net impurity concentration on both sides of the junction and the junction area, A_c. As the impurity concentration increases, the junction depletion layer decreases, and the capacitance increases.

The *punch-through voltage*, V_{pt}, (i.e., the voltage at which the collector space-

Fig. 1—Geometry of the 2N1708 planar epitaxial silicon transistor.

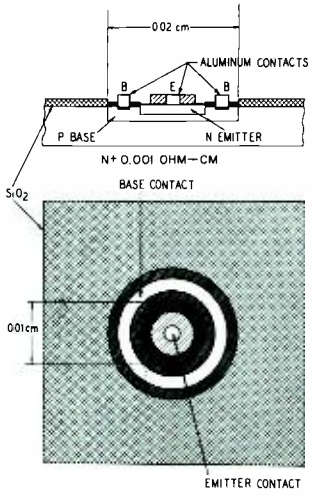
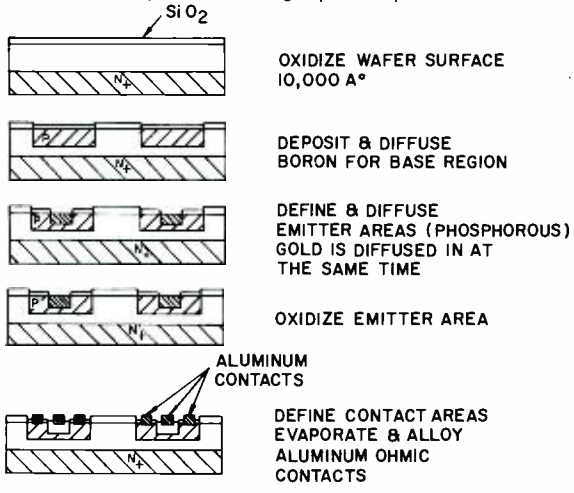


Fig. 2—Processing steps in fabricating a planar epitaxial silicon transistor.



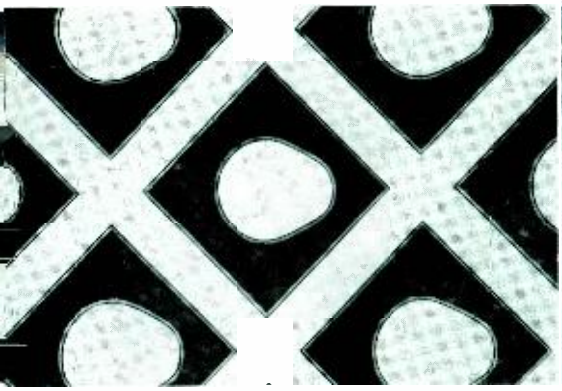


Fig. 3b—Emitter pattern defined in base area (abt. 400x).

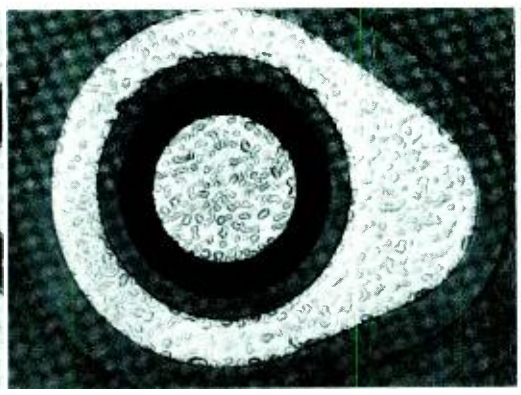


Fig. 3c—Defined metallized areas in emitter and base pattern, illustrating edge definition required to optimize device parameters (abt. 1400x).

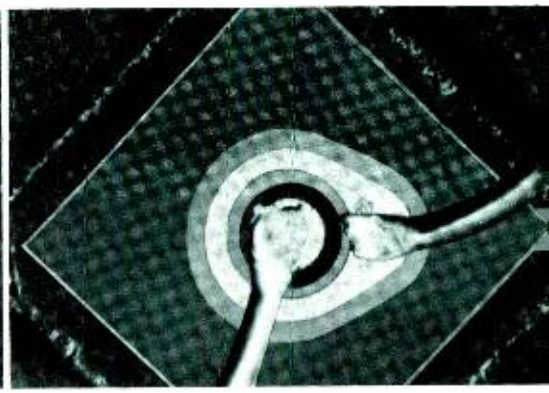


Fig. 3d—Thermo-compression bonded 2N1708 (abt. 1000x).

charge layer reaches the emitter region), is determined by the number of uncompensated impurities under the emitter. The larger the number of impurities, the higher the punch-through voltage.

The *cutoff frequency*, f_t, is determined primarily by the time required for a carrier to traverse the base region and the time to charge the collector capacitance in series with the collector resistance. The epitaxial device is somewhat faster because both C_c and the collector spreading resistance are reduced.

The time required to turn the transistor on (to increase the collector current to 90 percent of its final steady-state value) consists of two elements: the *delay time*, T_D, and the *rise time*, T_r. The time T_D is essentially that required to charge the emitter and collector capacitances and, for fixed circuit conditions, is dependent on the junction capacitances C_r and C_c. In a given circuit, the rise time and fall time are a function of the base carrier transit times and the current transfer ratio, h_{fe}. The higher the cutoff frequency, therefore, the shorter the rise and fall times are for a given h_{fe} value.

The *storage time*, T_s, in double-diffused transistors is a result of the injection of minority carriers into the collector region. Introduction of a recombination center such as gold decreases the lifetime, τ_c, and consequently the stored charge. It will be shown that epitaxial devices have considerably less stored charge at high current densities.

The *current transfer ratio*, h_{fe}, is determined by the ratio of the number of carriers collected at the collector junction to the number emitted by the emitter junction. A narrow base-width and high carrier lifetime in the base are, therefore, important for high current gain.

Table I — 2N1708 Description

Collector Area A_c	3.2×10^{-4}cm²
Emitter Area A_e	7.8×10^{-5}cm²
Base Width W	0.75×10^{-4}cm
Depth of Collector-Base Junction X_2	1.75×10^{-4}cm
Base Sheet Resistance R_s	400 ohms/square
Thickness of High-Resistivity Collector Region W_c (approximate)	5×10^{-4}cm
Collector-Region Resistivity P_c (after all diffusion steps)	1 ohm − cm
Gradient at Collector-Base Junction a_c	4×10^{20}cm^{-4}
Gradient at Emitter-Base Junction a_e	10^{23}cm^{-4}

IMPROVEMENT DUE TO THE EPITAXIAL STRUCTURE

Table II indicates some areas of modest improvement which are obtained when the thickness of the collector body is reduced by a factor of 10 and the impurity concentration in the collector is decreased by 20 percent. Two parameters, however, show considerable improvement: the collector-to-emitter voltage drop in saturation, $V_{ce}^{(sat)}$, and storage time, T_s. Fig. 5 shows V_{ce} as a function of collector current for the epitaxial and non-epitaxial devices. At high current levels, the voltage required to maintain a given collector current is considerably reduced for the epitaxial

Table II—Typical Electrical Characteristics of a Double-Diffused Epitaxial Transistor (2N1708) and a Similar Non-Epitaxial Transistor (2N708) Measured Under the Same Operating Conditions

Characteristic	2N708	2N1708	*Most Significan Parameters Affecting the Characteristic*
Junction Breakdown Voltage V_{cbo} (10 μa)	45 v	55 v	$\frac{1}{\lvert N_D - N_A \rvert}$
Saturation Collector-to-Emitter Voltage V_{ce} (sat) (I_c=50ma, I_b=10ma)	0.9 v	0.3 v	$I_c R_{sc}$
Base-to-Emitter Voltage V_{be} (I_c=10ma, I_b=1ma)	0.78 v	0.78 v	$\phi_c + R_b' I_b$
Collector Junction Capacitance C_c (V_{cb}=10v)	6 pf	5 pf	$A_c \mathscr{E} \lvert N_D - N_A \rvert$
Punch-through Voltage V_{pt}	>45 v	>55 v	$\int_{xe}^{kc} (N_D - N_A) dx$
Cutoff Frequency, f_T (V_{cc}=5 v, I_c=10ma)	300 Mc	330 Mc	$\frac{1}{2\pi\left(\frac{W^2}{2D} + R_{SC} C_C\right)}$
Delay Time, T_D (R_L=220Ω, V_{cc}=3 v, I_c=10ma I_{b1}=3ma)	6×10^{-9}sec	5×10^{-9}sec	C_e and C_c
Rise Time, T_r (R_L=220Ω, V_{cc}=3v I_c=10ma I_{b1}=3ma)	11×10^{-9}sec	9×10^{-9}sec	h_{fe} and $\frac{1}{f_T}$
Fall Time T_f (R_L=220Ω, V_{cc}=3v I_c=10ma, I_{b2}=1ma)	15×10^{-9}sec	12×10^{-9}sec	h_{fe} and $\frac{1}{f_T}$
Storage Time T_s ($I_c = I_{b1} = I_{b2}$= 10ma)	20×10^{-9}sec	18×10^{-9}sec	$\frac{\tau_c}{\frac{D\tau_b}{w^2}}$
h_{fe} (I_c=10ma, V_{ce}=1v)	45	50	

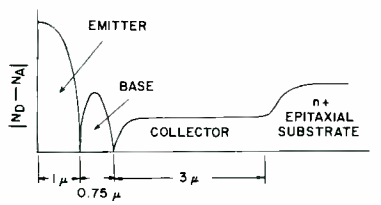


Fig. 4—Net impurity distributions for the 2N1708.

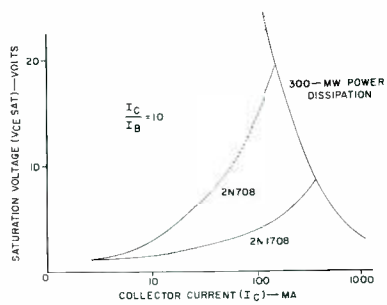


Fig. 5—V_{ce} as a function of collector current for an epitaxial and non-epitaxial silicon transistor.

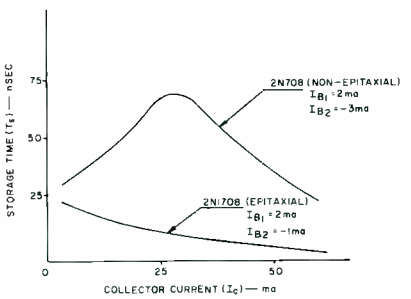
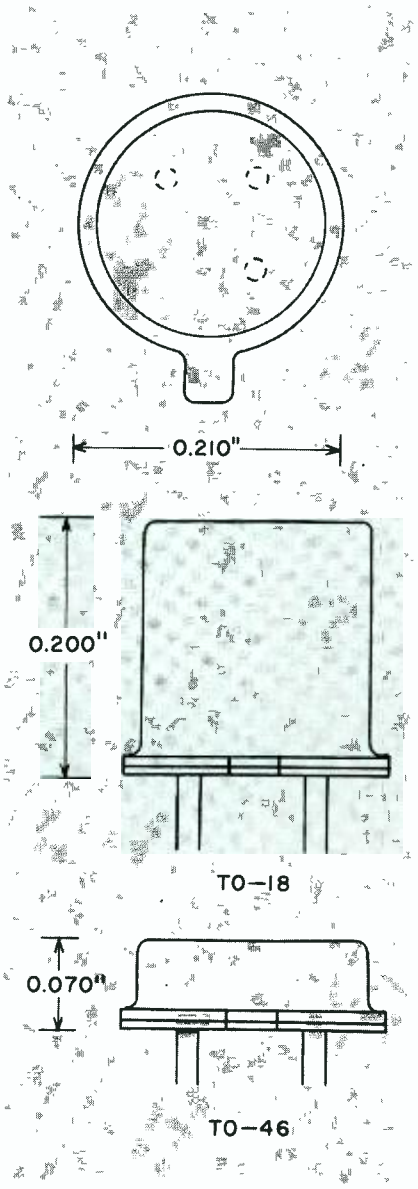


Fig. 6—Storage time as a function of collector current for an epitaxial and a non-epitaxial silicon transistor.[3]

transistor. Because the power dissipated in a transistor is the product of the V_{ce} and the collector current, it is obvious that for the same collector current, the power dissipated in an epitaxial transistor is substantially less than that in a non-epitaxial device.

Fig. 6 shows stored charge as a function of collector current[3] for the two structures. At low currents, storage time T_s is comparable. As the current increases, T_s decreases for the epitaxial unit, but increases and then decreases for the non-epitaxial device. As a result, the useful operating range of the transistor is greatly extended with the epitaxial structure. The low collector spreading resistance for the epitaxial structure is believed to be responsible for the lower carrier injection into the collector region at high current levels.

Fig. 7—TO-18 and TO-46 cases used for epitaxial transistors.



IMPROVEMENTS DUE TO NEW PACKAGING TECHNIQUES

Trends in miniaturization and the decreased power dissipation of the epitaxial devices indicated the need for a package smaller than the original TO-18 case. Fig. 7 shows the outlines was developed for these devices. The TO-46 case decreases the volume to less than half that occupied by the TO-18 case. Fig. 6 shows the outlines of the two cases.

SUMMARY

The double-diffused planar epitaxial silicon transistor switch described here shows improvement in most characteristics compared with the double-diffused planar type. Major improvements are obtained in the saturation voltage, high current stored charge, and current handling capabilities.

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DR. HAROLD S. VELORIC received the BA from the University of Pennsylvania in 1951, and the MS and PhD from the University of Delaware in 1952 and 1954, respectively. He joined the Technical Staff of Bell Telephone Laboratories in Murray Hill, N.J. in 1954, and was engaged in the development of various types of silicon diodes, including power rectifiers, voltage-regulating diodes, computer diodes, and solar cells. Since joining the RCA Semiconductor and Materials Division in Somerville, N.J., in 1958, he has headed RCA design and development work on silicon computer devices. He is responsible for engineering development of all high-frequency silicon switching transistors, as well as all computer silicon devices. Dr. Veloric has published a number of technical papers. He is a member of the American Chemical Society, the Electrochemical Society, and the Institute of Radio Engineers.

HENRY KRESSEL received the BA in Physics *magna cum laude* from Yeshiva College in 1955, and the MS in Applied Physics from Harvard University in 1956. In 1959, after completing U.S. Army service, he received the MBA degree in Industrial Management from the Wharton School of the University of Pennsylvania. After graduation he joined the Burroughs Corporation, Great Valley Laboratory, as a staff engineer. In October of 1959, he joined the RCA Semiconductor and Materials Division at Somerville, N.J., as a computer-device design engineer. In this capacity he was instrumental in the development of many of the basic processes for the fabrication of silicon mesa, planar, and planar epitaxial transistors. Since 1960 he has been Project Leader of the Microwave Diode group in the GaAs Product Development activity, where he is presently responsible for design, development, and pilot-line engineering of variable-capacitor microwave diodes. Mr. Kressel is a member of the I.R.E. and the Electrochemical Society.

DR. ADOLPH BLICHER received the BSEE from the University of Toulouse, France, and the MS in Electrical Communications from École Superieure d'Electricté, Paris, France. In 1938, he received the ScD in Physics from the Technical University of Warsaw, Poland. Before coming to the United States in 1946, he was connected with the electronics industry in Poland. He has been active in the semiconductor field in this country since 1954, and has been associated with the RCA Semiconductor and Materials Division since 1955. As Manager of Computer-Device Development, he was responsible for development of a wide variety of silicon and germanium transistors and diodes. He is presently Manager of Gallium Arsenide Product Development. Dr. Blicher has authored numerous technical publications and is a Senior Member of the IRE and a Member of the Electrochemical Society.

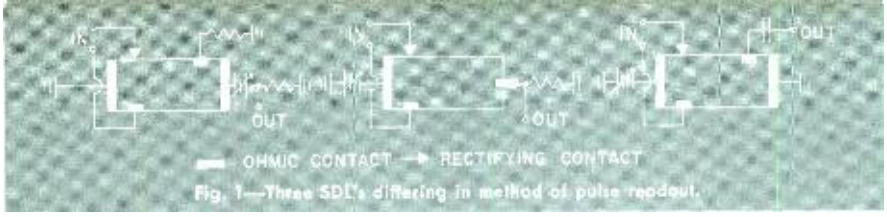

Fig. 1—Three SDL's differing in method of pulse readout.

THE SEMICONDUCTOR DELAY LINE

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Systems Laboratory
Surface Communications Division
DEP, New York, N. Y.

THE SEMICONDUCTOR DELAY LINE[1,2] (SDL) is an active circuit element with an electronically variable delay and a high per-unit-volume performance. It utilizes the time of propagation of an excess-minority-carrier pulse along a filamentary transistor, differing from the latter in that it requires a localized sensor to effect pulse readout.

Small size and simplicity make the SDL (Fig. 1) applicable to integrated electronic structures where in addition to use as a delay element, it can be combined in numbers to yield other functions.[3,4,5] Its electronically variable delay, coupled with possible signal gain, makes it versatile — as a tuneable oscillator[6], a frequency converter[7], or a frequency or phase modulator[6].

Against these advantages must be weighed its relatively low delay-to-rise-time ratios and requirement for a voltage supply. However, the small size extenuates to some extent the poor figure of merit per device; at comparable levels of signal attenuation and at comparable delays in the range of 1 to 100 μsec, the SDL bit-storage density is two to four orders of magnitude higher than in the commercial acoustic or electromagnetic delay lines.

CHARACTERISTICS

The delay-to-rise-time ratio and the maximum bit storage of the SDL at any given temperature and attenuation level are a function only of the voltage across the SDL (Fig. 2). At frequency cutoff, delay-to-rise-time ratios of about 20 are obtainable with a drift bias of 100 volts at room temperature. The maximum number of pulses storable under the same conditions is about six. Pulse storage per device increases directly as the square root of pulse amplitude attenuation (in db) due to carrier diffusion. With presently available materials, the SDL can provide delays ranging from fractions of a microsecond to about a millisecond.

Unlike acoustic delay lines, the SDL has a lowpass frequency response. For square-pulse inputs and low injection levels, the output pulses are symmetrical and approach a Gaussian shape for appreciable amplitude attenuation by carrier diffusion. For a given delay line and a given input pulse, the delayed pulse amplitude and rise time are functions of the delay time.

Specification of maximum delay time and minimum delay/rise-time ratio at frequency cutoff are sufficient to determine the length of the delay line. The smallest feasible device cross-section is determined for a given maximum delay by the requirement that the surface recombination lifetime be long compared to the delay time.

Fig. 2—Significant SDL relationships.

RESPONSE TO A SQUARE PULSE:

$$t = \frac{L^2}{uV} \qquad \Delta_c = 39\sqrt{\frac{V}{T}}$$

$$t_{pc} = \frac{t}{\Delta_c} \qquad N_c = \frac{1}{3}\Delta_c$$

RESPONSE TO A SINUSOIDAL SIGNAL

$$f_c = 10\,\frac{u}{L^2}\sqrt{\frac{V^3}{T}} \qquad N_c = 10\sqrt{\frac{V}{T}}$$

CUTOFF POINT (CP) DEFINED BY PULSE AMPLITUDE ATTENUATION OF 3 DB DUE TO CARRIER DIFFUSION.

t = DELAY TIME (SEC)
Δ_c = DELAY TO RISE TIME RATIO AT CP
f_c = CUTOFF FREQUENCY (CPS)
t_{pc} = CUTOFF PULSE DURATION (SEC)
N_c = NUMBER OF PULSES STORABLE AT CP
u = AMBIPOLAR MOBILITY (CM^2/VOLT-SEC)
T = TEMPERATURE (^oK)
L = EFFECTIVE LENGTH OF DELAY LINE (CM)
V = VOLTAGE ACROSS L (VOLTS)

MATERIALS AND RESULTS

High-resistivity materials avoid excessive heating at the large biases at which the SDL normally operates. Of course, a reduction in the level of steady power dissipation means a corresponding decrease in the maximum feasible signal level. The carrier lifetime should be long relative to the delay time. Given the delay and the corresponding delay to rise time ratio at frequency cutoff, the lower the ambipolar mobility the shorter the device, and accordingly, the higher the power dissipation per unit volume.

Since the SDL geometry makes a reverse-biased p-n collector inefficient, and because the heating associated with the making of a p-n junction leads to carrier lifetime degradation (and in high-resistivity materials to nonuniform resistivity changes) it would seem advisable to effect pulse readout through conductivity modulation. The pulse is then sensed by a proper arrangement of ohmic contacts on the semiconductor filament, and pulse injection may be accomplished with a rectifying metal-to-semiconductor contact (Fig. 1). All contacts may be made with an ultrasonic welder or by electroplating. The whole process is simple and leaves the properties of the material unaltered.

Experimental SDL's were made by the above technique from high-resistivity p-type silicon (Figs. 3, 4). Delays in the range of 10 to 500 μsec with delay-to-rise-time ratios of up to 15 have been measured in these lines, at attenuations of 0 to 20 db. Typical dimensions of a line providing a delay of 200 μsec, variable within ±50 percent would be 0.3 by 0.3 by 3 cm.

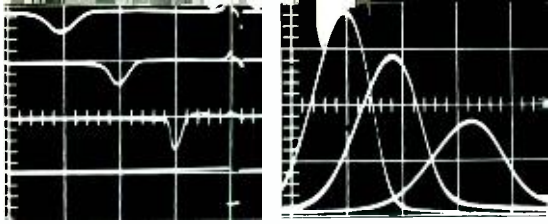

Fig. 3—Experimental SDL input pulse and corresponding delayed pulse vs. delay. Vertical scale for each trace: Reading down, 2, 1, 0.5, 0.2 v/sq. Horizontal scale 100 μsec/sq.

Fig. 4—A delayed pulse vs. voltage across the SDL delays of 240, 285, 350 μsec corresponding to biases of 48, 41, 33 volts, respectively. Vertical scale, 0.05 v/sq. square. Horizontal scale, 50 μsec/sq. Input is 3-v, 30-μsec square pulse.

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JOHN J. SEIN graduated from Union College in 1956 with a BS in physics. He continued his studies at Yale University where he received an MS in 1958. Since 1960, he has been a Member of the Technical Staff at the SurfCom Systems Laboratories, engaged in the development of semiconductor signal-processing devices and thin-film circuits.

DR. SUMNER N. LEVINE received a BS from Brown University (1946) and a PhD from the University of Wisconsin (1949). He taught at the University of Chicago (1949-1950) and Columbia University (1950-1954). Subsequently, he headed the Research Laboratories of the U. S. Veterans Administration (1954-1956) at East Orange, N. J. and later directed the Chemistry, Physics, and Metallurgy Laboratories at American Machine and Foundry, Greenwich, Conn. (1956-1958). Since 1958, with RCA, he has been at the DEP SurfCom Systems Lab., directing advanced devices research and development. He is now on leave, serving as Chairman of the Materials Sciences and Professor of Engineering at the new College of Engineering, State University of New York, Long Island Center. Dr. Levine has authored about 42 technical papers and has edited and contributed to two books, *Modern Techniques of Energy Conversion*, Dover (1961) and *Solid State Microwave Amplifiers* (Dover, in press).

J. J. Sein (l.) and Dr. S. N. Levine ▶

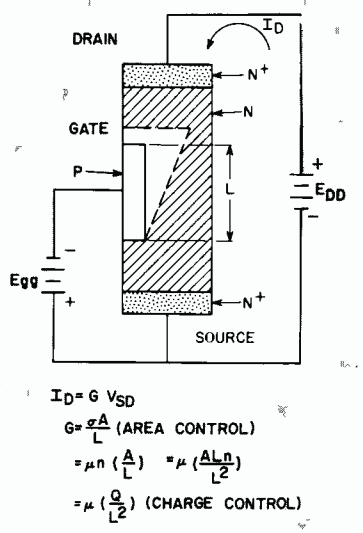

Fig. 1—Basic unipolar transistor.

UNIPOLAR TRANSISTORS

Unipolar transistors offer new freedom in circuit design—high input impedance compared with bipolars and low noise characteristics, and they can be designed for linear or nonlinear applications. Basic unipolar concepts, and characteristics of an important new developmental diffused unipolar transistor are presented herein.

L. KRASSNER, J. OLMSTEAD, and J. SCOTT

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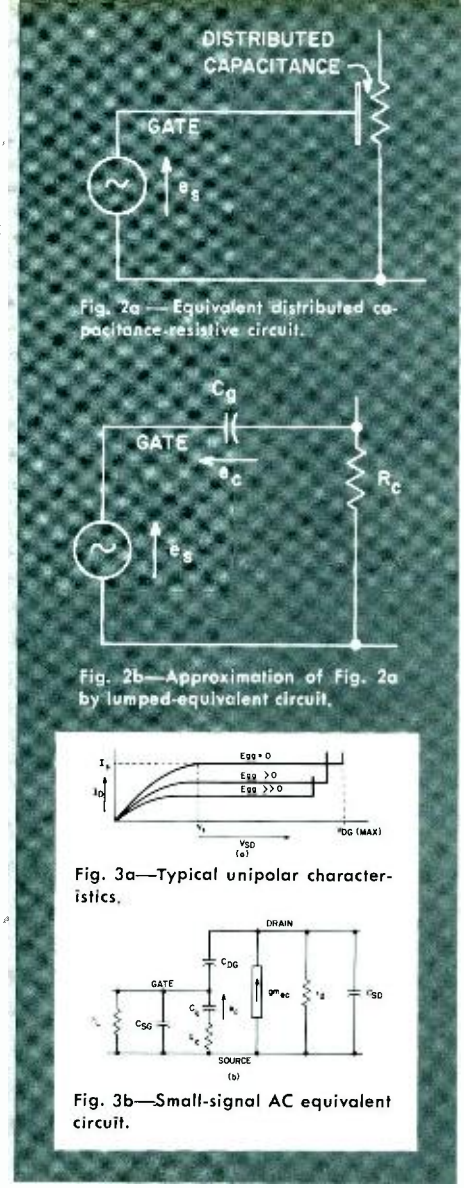


Fig. 2a — Equivalent distributed capacitance-resistive circuit.

Fig. 2b—Approximation of Fig. 2a by lumped-equivalent circuit.

Fig. 3a—Typical unipolar characteristics.

Fig. 3b—Small-signal AC equivalent circuit.

ALTHOUGH THE operating principles which are the basis of the unipolar or field-effect transistor were first recognized[1] in 1935, it wasn't until 1948 that Shockley and Pearson[2] proposed application of these principles to semiconductor devices. In 1952, Shockley[3] described the unipolar transistor in its present form and developed the basic equations which define its operation. Except for exploratory experiments[4], the device was not further developed until the recent expansion of semiconductor technology.

BASIC CONCEPTS

The unipolar transistor is basically a modulated resistor (Fig. 1). In its simplest form, the device consists of: 1) the *source* where carriers enter; 2) the *drain* where carriers leave; 3) the *gate*, the area between the source and drain; and 4) the *channel*, or active portion of the transistor beneath the gate.

The function of the gate is to vary the resistance from source to drain. If a voltage E_{gg} is applied between the channel and the gate in a direction which reverse-biases this junction, the depletion region expands into the channel and increases the resistance of the channel.

The drain current I_D and source-to-drain voltage V_{SD} are related through the conductance G of the device:

$$I_D = GV_{SD} \qquad (1)$$

(For simplicity, the conductance G is assumed to be totally within the active region of the device, i.e., in the channel.)

The conductance of the channel may be expressed in terms of conductivity σ, cross-sectional area A, and channel length L:

$$G = \left(\frac{\sigma A}{L}\right) \qquad (2)$$

Varying any of these parameters changes the value of G and, thus, varies I_D, V_{SD}, or both. In the unipolar transistor, G is modulated through variations in the cross-sectional area of the active region A that result from changes in the gate depletion layer.

A further extension of the expression for G into still more fundamental terms describes the charge-control concept. Conductivity σ can be re-expressed as the product of mobility μ and mobile charge-carrier density n; after rearrangement, the product ALn can be replaced by the total mobile charge Q:

$$G = \mu n \left(\frac{A}{L}\right) = \mu \left(\frac{ALn}{L^2}\right) = \mu \left(\frac{Q}{L^2}\right) \qquad (3)$$

Thus, since modulation of Q results in modulation of G, the control electrode (the gate) is simply one plate of a capacitor to which mobile charge is transferred, stored, and made inactive. Although these two modulation concepts (area control and charge control) are essentially the same, each has certain merits in explaining unipolar operation.

The upper frequency response of a unipolar transistor is limited by either the charge transit time-constant or the internal input time-constant. Johnson and Rose[5] have shown that under ideal conditions, these time constants are equal. In practice, however, the input time-constant is dominant because of an excess of nonactive capacitance built into the device. The origin of the input time-constant may be shown by replacing the gate diode with an equivalent distributed capacitance-resistive circuit (Fig. 2a). This distributed circuit may, in turn, be approximated by a simpler lumped-equivalent circuit (Fig. 2b). According to the charge-control concept, the signal voltage appearing across the capacitor is the important modulation parameter and may be expressed as:

$$e_c = e_s \left[\frac{1}{1 + j\omega R_c C_g}\right] \qquad (6)$$

Where: e_s = applied input signal; e_c = portion of this signal appearing across C_g; and R_c = equivalent series channel resistance. The value of e_c is approximately equal to the value of e_s when $\omega R_c C_g$ is much less than 1, and e_c is equal to 0.707 e_s when $\omega R_c C_g$ has a value of 1. The relationship establishes the upper half-power frequency of the unipolar transistor and results in a frequency falloff of 6 db/octave above this frequency. (It is assumed that the lumped equivalent input circuit is a fair

Fig. 4—Oxide-masking–photoresist fabrication steps.

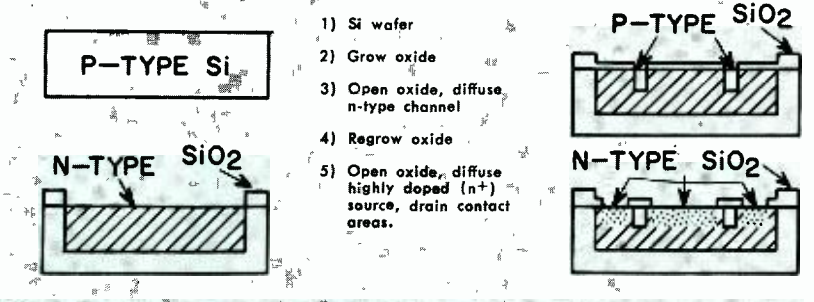
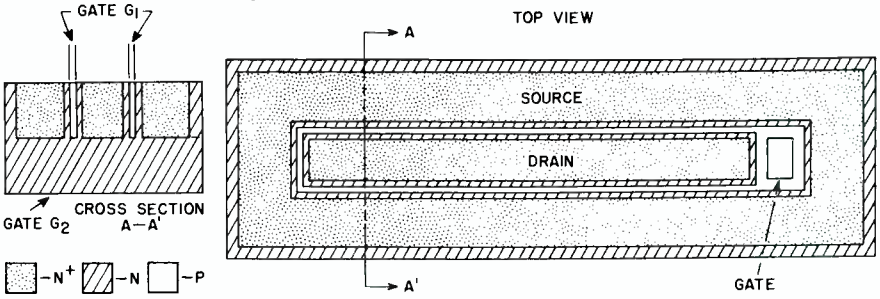
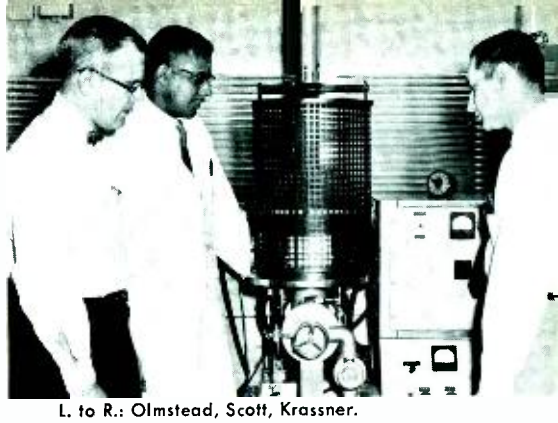


Fig. 5—Device during contact-area formation.





L. to R.: Olmstead, Scott, Krassner.

approximation of the true distributed case.)

A secondary effect associated with the input time-constant appears in the input impedance of the device. Normally, the unipolar transistor is a high-input-impedance device; however, at frequencies approaching the upper half-power frequency, input impedance falls quite rapidly. This drop includes the expected reactance drop as well as a real component drop resulting from the equivalent series channel-resistance. Thus, the Q of the input circuit decreases rapidly at these frequencies, and input circuits become heavily loaded.

The typical characteristic curves for a unipolar transistor shown in Fig. 3a are similar to the characteristic curves of a pentode vacuum tube. Fig. 3b shows a small-signal AC equivalent circuit.

DEVICE FABRICATION

The developmental diffused unipolar transistors described in this paper were made by a conventional oxide-masking photoresist technique (Fig. 4).

Formation of the Channel

In this process, a silicon wafer (polished on one side and properly cleaned) is subjected to high-temperature oxidation in order to form the diffusion mask for the channel diffusion. After conventional photoresist and etching processes open up the oxide in small rectangles, the channel is diffused by firing the wafer in a high-temperature furnace in an atmosphere containing the proper dopant.

Formation of the Gate

Because the mask for the gate diffusion is grown during the last portion of the channel-diffusion step, photoresist techniques can be applied immediately and the oxide opened in a loop configuration for the gate diffusion. Normal two-zone diffusion techniques are again applied to complete gate-region formation.

Formation of Contact Areas

After the gate diffusion step, a thermal oxide mask is regrown. The mask is opened in areas adjacent to the gate, but not in contact with it. These areas are then diffused to yield highly doped, low-resistance contact areas. These areas do not touch the gate region; a buffer region of less-doped material is left between the contact areas and the gate. Thus, reverse breakdown voltages are not affected by this step. A top view of the device at this stage is shown in Fig. 5. Photoresist techniques are used to open contact areas in the oxide, and aluminum is evaporated over the openings. The device is then diced, mounted, thermal-compression bonded, encapsulated, and tested.

Differences from Simplified Model

Practical unipolar transistors differ from the simplified model previously discussed in that they contain two distinct gate regions that are electrically separate. One gate, the purposely diffused loop configuration, is highly doped; hence, its depletion region moves primarily into the channel rather than back into the gate. As a result, this gate has very effective control properties. The other gate, the original silicon substrate, is lightly doped; hence, its control properties are less effective. The importance of these two gates lies in their interaction through a feedback phenomena and possible use as separate input circuits.

CHARACTERISTICS

In the static source-drain characteristics of a developmental unipolar transistor (Fig. 6a), both gates are driven. Saturation current is about 23 ma, and saturation voltage approximately 5 volts. The curves do not indicate the higher drain-voltage region; diode breakdown limits this voltage to 28 volts. In Figs. 6b and 6c, the characteristics are shown for gate *1* driven (gate *2* tied to source) and gate *2* driven (gate *1* tied to source), respectively; the values for saturation current and voltage do not change. Gate *1* is

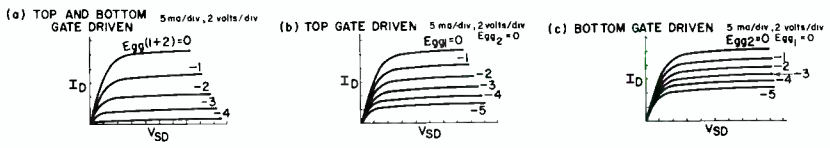


Fig. 6—Static source-drain characteristics, developmental unipolar transistor.

LOWELL A. KRASSNER received the BS in physics from MIT in June 1958 and is presently pursuing graduate studies in physics at Stevens Institute of Technology. From 1958 until July, 1959, he was employed at the U.S. Army Signal Research and Development Laboratory-Fort Monmouth, N. J., in the development and measurement of solid-state infrared detectors. He joined the Semiconductor and Materials Division in August 1959, and has worked on GaAs solar cells and varactor diodes encompassing all aspects of device fabrication. Since August 1960, he has been working on advanced techniques of device processing in connection with the development of silicon unipolar transistors.

JOHN A. OLMSTEAD received his BSEE from the University of Buffalo in 1952, and his MSEE from Newark College of Engineering in 1957, and completed the required courses for an MS in Mathematics from the University of Buffalo in 1960. He joined RCA as a specialized trainee in 1952, and was eventually assigned to the Receiving Tube design group at Harrison. In 1953 he joined the RCA Laboratories in Princeton to work on gaseous electronics. He returned to Harrison in 1954 to work on specialized industrial tubes. Between 1958 and 1960 he was an Assistant Professor of EE at the University of Buffalo. During the summer of 1959 he worked at the Semiconductor and Materials Division on GaAs solar cells. When he returned to Somerville in mid-1960, he formed a new group to work on advanced silicon devices, such as unipolar transistors. In conjunction with J. Scott, he developed a very powerful solid-to-solid diffusion technique. He is the coinventor of a unipolar transistor having transconductance decreasing linearity with gate voltage. Mr. Olmstead is a member of the IRE and Sigma Xi.

JOSEPH H. SCOTT received the AB in chemistry from Lincoln University in June 1958. He attended Howard University Graduate School of Chemistry and is presently attending Stevens Institute of Technology Graduate School of Physics. In July, 1959, he joined the Semiconductor and Materials Division, and has worked on the development of GaAs varactor diodes, and contributed notably to the development of high-efficiency GaAs solar cells. As a member of a new group in advanced silicon devices, he has worked on diffusion and contamination. In collaboration with J. Olmstead, he developed a solid-to-solid diffusion technique which has been instrumental in the fabrication of devices such as the unipolar transistor. Mr. Scott is a member of the Electrochemical Society.

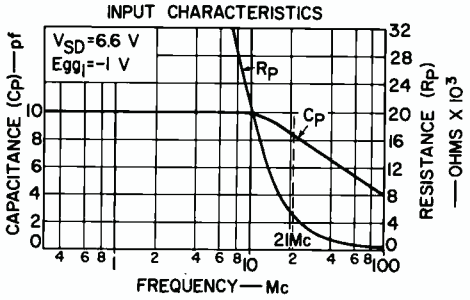


Fig. 7—Input characteristics.

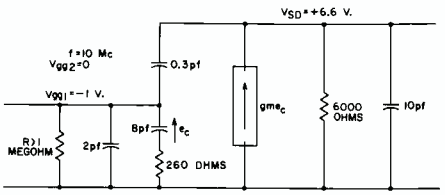


Fig. 8 — Resistance and capacitance of an equivalent circuit.

more effective in its control properties, although the feedback effect between these gates decreases the difference. In addition to the difference in gate effectiveness, there is a difference in gate cutoff voltage, the voltage that must be applied to the gate to reduce the drain current to zero. This difference can be of considerable importance in designing useful devices because it allows the saturation voltage and the gate cutoff voltage to have different values.

The input impedance for gate *1* (gate *2* tied to source) was measured with a Boonton RX meter, which indicates the equivalent parallel resistance and capacitance (Fig. 7). When these values are converted to true series resistance-capacitance circuit parameters, the values are constant to above 100 Mc.

Output impedance was also measured on a Boonton RX meter. The output circuit consisted of a 6000-ohm resistance shunted by a 10-pf capacitance. A good correlation exists between the measured output resistance and the slope of the curve of drain voltage as a function of drain current. This resistance is lower than desired because it limits the maximum voltage gain available from the unit to 35. Further analysis of the factors influencing this parameter must be undertaken for future designs. The high output capacitance is a result of grounding the back gate, which has considerable drain-to-gate capacitance.

Resistance and capacitance values of an equivalent circuit are shown in Fig. 8. The operating conditions listed are typical for many circuit applications.

The variation of transconductance as a function of applied bias is shown in Fig. 9. The linearity of this relationship is of considerable interest because it represents the desirable square-law device sought for many years. Such devices possess almost perfect multiplication characteristics (modulators, demodulators, etc.). This transconductance-bias relationship is a result of device design in which the depletion region of the gate moves into a nonuniformly doped channel. This type of channel has been studied in great detail. Fig. 10 shows that control of the channel-doping profile makes it possible to obtain specific transfer characteristics for particular applications. The frequency response of a typical unipolar (Fig. 11) has an upper half-power frequency of 21 Mc.

FUTURE APPLICATIONS

To the application engineer, the unipolar transistor offers new freedom in circuit design. The device has a high input impedance compared with bipolar transistors, low noise characteristics, and can be designed for linear or nonlinear applications.

The similarity of the characteristics of unipolar transistors and vacuum tubes (Table I) makes it possible to modify many existing vacuum-tube circuits for unipolar applications, thus gaining the advantages of a solid-state device. Desirable unipolar features are:

1) *Low Noise:* Noise measurements, as yet incomplete, indicate that the unipolar transistor is a low-noise device. Noise figures below 1 db are easily obtained at 200 kc. Although the noise behavior at other frequencies has not been thoroughly investigated, the unipolar transistor seems promising for the front stages of high-gain amplifiers.
2) *High Input Impedance:* Input impedances over 100 megohms (without feedback) are readily obtained at frequencies below the upper half-power frequency. As a result, the devices may be used in high-input-impedance stages and impedance-matching interstages.
3) *No Offset Voltage:* Because the unipolar transistor contains no offset voltage, it is useful in computer applications, such as analog-to-digital conversion and direct-coupled circuits.
4) *Designed Nonlinearity:* The unipolar transistor can be designed with various transfer characteristics (i.e., various forms of nonlinearity). The device previously described shows almost perfect square-law characteristics; remote- and sharp-cutoff devices are theoretically and technically feasible. Thus, multiplication (modulation and demodulation) and amplification with various AGC characteristics are possible.

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Table I—Comparison of Electrical Properties of Unipolar Transistor and 6AU6 Pentode Vacuum Tube

Characteristic	*Unipolar Transistor*	*Pentode Vacuum Tube*
Heater Power, ω	None	1.89
Input Capacitance, pf	8	5.5
Feedback Capacitance, pf	0.3	0.004
Output Capacitance, pf	10	5
†Supply Voltage (min.), v	6	40
Current Drain (max.), ma	23	17 + 4*
Transconductance (max.), μmhos	6000	5800
Output Resistance, ohms	6000	1 x 10^6
‡Input Resistance, ohms	1 x 10^6	1 x 10^6
¶Cutoff Frequency F (3 db), Mc	23	100
Noise, db	1	4.5

*17 plate current; 4 screen-grid current
†To operate in desirable saturation region
‡Normally circuit limitation
¶Simple circuitry

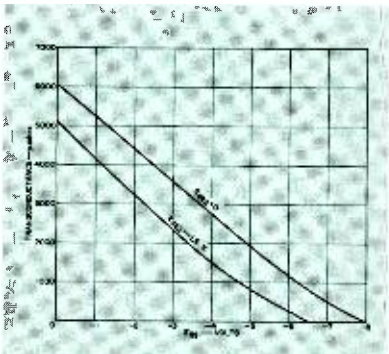

Fig. 9—Transconductance vs. applied bias.

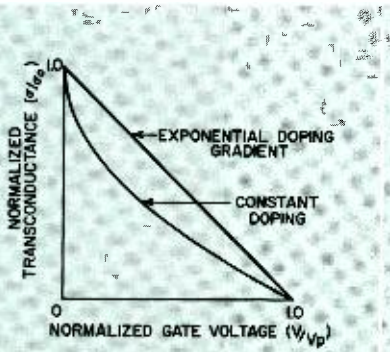

Fig. 10 — Normalized transconductance vs. normalized gate voltage.

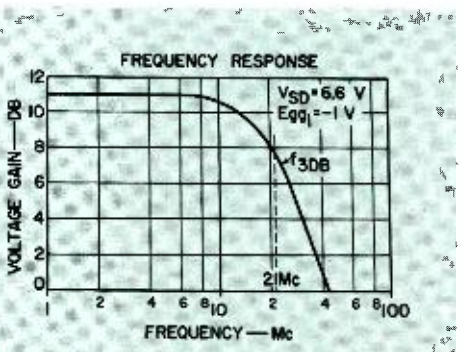

Fig. 11—Frequency response.

GALLIUM ARSENIDE VARACTOR DIODES

This new small-area diffused-junction GaAs varacter diode has typical cutoff frequencies over 250 Gc, and is designed for low-noise parametric amplifiers. Circuit-performance gain, bandwidth, and noise figures are outstanding.

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SEMICONDUCTOR variable-capacitance diodes have become increasingly important in applications such as parametric amplification and subharmonic and harmonic frequency generation. Varactor diodes with satisfactory characteristics have been available for frequencies approaching the microwave region, but the absence of suitable diodes for higher frequencies has hampered efforts to seek out new (higher) frequency communication bands.

The small-area diffused-junction GaAs varactor diode described here is designed for use in low-noise parametric amplifiers. Results of application studies are also included because the data obtained were useful in achieving the optimum design of the diode.

VARACTOR-DIODE EQUIVALENT CIRCUIT

The optimum performance of a varactor diode depends to a large extent upon the physics of the device. In Fig. 1, the junction is constructed by solid-state impurity diffusion into a substrate. The mesa varactor structure shown was chosen because of its inherently superior mechanical stability as compared with point-contact structures. It is possible that further improvement might be obtained with epitaxially grown layers, but data on these structures are not yet available.

The equivalent circuit of the varactor diode shown in Fig. 2 includes the electrical properties of both the junction and the package. The capacitance and inductance of the package are assumed to be constant over a wide temperature range. The dissipative resistance of the package is a function of frequency; although it is negligible at low frequencies, it becomes appreciable in the microwave frequency range.

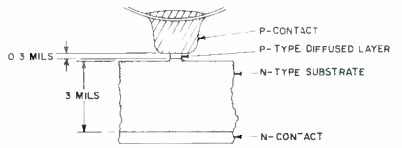

Fig. 1—Varactor diode.

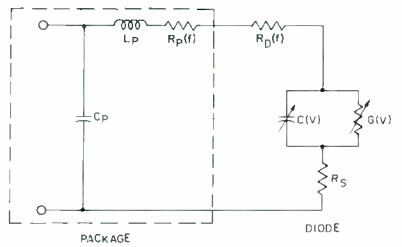

Fig. 2—Equivalent circuit.

The diode series resistance $R_d(f)$, also a function of frequency, is the sum of the resistances of the semiconductor material on both sides of the junction and the contact resistances. Although $R_d(f)$ decreases slightly at elevated temperatures, it is assumed to be constant over the temperature range considered to simplify the analysis.

Because the package capacitance C_p and inductance L_p are lossless elements, they are not considered in the evaluation of the varactor diodes. The package dissipative resistance $R_p(f)$ is included because it can seriously limit performance if it is excessively high.

The total series dissipative resistance $R_s(f)$, therefore, is the sum of the package and diode resistances:

$$R_s(f) = R_p(f) + R_d(f) \qquad (1)$$

This quantity will be used in the evaluation of the quality factor Q.

The equivalent circuit of the diode itself is represented by the series resistance $Rd(f)$ in series with the parallel arrangement of the junction capacitance $C(V)$ and the junction shunting conductance $G(V)$. (The two latter quantities are functions of voltage.) A high-performance diode for the microwave frequency range must have a junction capacitance $C(V)$ of the order of 1 pf or less. Therefore, the junction shunting conductance $G(V)$ is negligible in the reverse-bias region, and the reverse current is small over the dynamic range employed as compared to the component of current through the capacitance in the microwave frequency region. The equivalent circuit of the diode alone can thus be considered as a series resistive-capacitive circuit.

VARACTOR-DIODE FIGURES OF MERIT

From the various groups working with parametric amplifiers within RCA, several figures of merit for predicting circuit performance have been evolved.

LEONARD H. GIBBONS, JR. received the BSEE from Johns Hopkins University in 1959, and is presently studying toward an MSEE at Rutgers University. He joined RCA the same year as a Design and Development Trainee and was subsequently assigned to the SC&M Division in Somerville, N. J. His early work included the fabrication and evaluation of GaAs varactor diodes and solar cells. After a leave of absence for service with the U. S. Army Ordnance Corps, he returned to the Advanced Devices activity in Somerville. In 1961, he transferred to the newly organized GaAs Product Development activity, where he is presently concerned with fabrication techniques and microwave evaluation of varactor diodes. Mr. Gibbons is a member of the IRE, Tau Beta Pi, and Eta Kappa Nu.

MICHAEL F. LAMORTE received the B.S. from Virginia Polytechnic Institute in 1950 and the M.E.E. from the Polytechnic Institute of Brooklyn in 1951. He held a Teaching Fellowship in 1950-51 and a Research Fellowship in 1951-52 at the latter institution. He was an Adjunct Professor in the E.E. Graduate School of University of Pittsburgh. From 1952 to 1955 he was at the Signal Corps Engineering Labs, Fort Monmouth, N. J., in study of fundamental properties of semiconductors. From 1955 to 1959 he was with the Westinghouse Electric Corp., investigating device theory and technology. Special contributions were made to high-power silicon devices, crystalline material and diffusion studies. In October 1959, he joined the RCA Semiconductor and Materials Division at Somerville, N. J. Now, as Project Leader of the New Devices Section, Advanced Development, he is responsible for R&D on varactor diodes and GaAs solar cells. Author of several papers, he is a member of the American Physical Society, the IRE and IRE-PGED, Phi Kappa Phi, Tau Beta Pi, and Eta Kappa Nu.

ALOIS E. WIDMER served an apprenticeship in electromechanics in the high-frequency field at Brown-Boveri, Baden, Switzerland, from 1946 until 1950. He then attended Engineering School, Zurich, Switzerland, and received a degree in Electrical Engineering in 1955. He was later an exchange student in London, England, and also an exchange employee to Thompson-Houston, Ltd., Rugby, England. From 1950 to 1960 he worked at Brown-Boveri, Baden, Switzerland, on high-power semiconductor devices, and came into contact with a wide variety of problems in the design and fabrication of semiconductor devices. In 1960 he joined RCA SC&M Advanced Development activity at Somerville, N. J. He has since been working on the development of GaAs varactor and switching diodes and high power rectifiers. He is presently engaged in the development of a GaAs switching transistor.

DEFINITION OF TERMS

A	Junction area, cm²	R_d	Diode series resistance, ohms, measured ta microwave frequencies.
C	Junction capacitance, farads	R_m	Resistance of semiconductor material, ohms
C_p	Package capacitance, farads	R_p	Package dissipative resistance, ohms
f	Operating frequency, cps	R_s	Total series dissipative resistance, ohms, measured at microwave frequencies.
f_{co}	Frequency cutoff, measured at microwave frequencies including package losses, cps	V_p	Pump voltage, volts
G_t	Total conductance, mhos	V_B	Breakdown voltage, volts
G	Junction shunting conductance, mhos	ω_s	Signal frequency, rad/sec
K	Constant in capacitance-voltage relation	r_m	Radius of mesa, cm
L_p	Package inductance, henries	x_j	Junction depth, cm
n	Exponent in capacitance-voltage relation	x_m	N-doped region of mesa
Q	Quality factor of diode	x_n	Base region of diode
Q_s	Quality factor of diode at signal frequency	ρ_n	Resistivity of n-region, ohm-cm
R_c	Contact resistance, ohms	ρ_p	Resistivity of p-region, ohm-cm
		ϕ_o	Built-in potential of diode, volts

The quality factor Q mentioned above is defined as:

$$Q(V,f) = \frac{1}{2\pi f R_s(f)\, C(V)} \qquad (2)$$

Q is defined for a particular frequency value and bias point. It is a function of frequency both explicitly and through the total series resistance $R_s(f)$; it is a function of voltage through the junction capacitance $C(V)$ at the bias point.

An alternate figure of merit which may be derived from Eq. 2 is the frequency for which Q is unity, or the cutoff frequency f_{co} at the bias point:

$$f_{co}(V,f) = \frac{1}{2\pi R_s(f)\, C(V)} \qquad (3)$$

This quantity is preferred by some investigators because it is not as strong a function of frequency as is Q.

There is no generally accepted voltage at which Q and f_{co} are evaluated. Uhlir[1] has suggested the point at which $C(V)$ is a minimum, i.e., the reverse breakdown voltage. In the evaluations reported in this paper, the more conservative −1 and −6 volts are used.

A third figure of merit is the exponent n used in the following junction capacitance-voltage expression[2]:

$$C(V) = \frac{K}{(\Phi_o - V)^n} \qquad (4)$$

Where: K is independent of voltage and Φ_o is the junction built-in voltage. The value of Φ_o is approximately 1 volt for the gallium arsenide diodes discussed in this paper. The constant K depends on the dielectric constant of the semiconductor material used, the impurity concentration, and the type of junction (abrupt or graded). The value of n is approximately ½ for abrupt junctions and ⅓ for graded junctions.

A fourth figure of merit is the capacitance ratio $\Delta C/C$, defined as: (5)

$$\frac{\Delta C}{C} = \frac{C_{(-1)} - C_{(-6)}}{C_{(-1)}}$$

This quantity is sometimes preferred by circuit-design engineers because it is easily measured and provides a convenient indication of junction characteristics in terms of a circuit parameter. Eq. 4 shows that the ratio $\Delta C/C$ is a function of both n and Φ_o at zero bias; there is a marked dependence on n, but relatively little on Φ_o. Table I lists values of $\Delta C/C$.

DIODE DESIGN CONSIDERATIONS

To achieve gain in a negative-resistance amplifier, it is necessary that the total conductance be negative. The total conductance G_t for a parametric amplifier is: (6)

$$G_t = -\frac{1}{2}\,\omega_s V_p \frac{dC}{dV} + \frac{\omega_s C}{Q_s}$$

Because the value of C is usually determined by the impedance level required in the circuit, it is desirable to make Q_s, V_p, and dC/dV relatively large.

To fabricate diodes having a high value of Q_s, it is necessary to make the capacitance and the diode series resistance small. The contribution of the semiconductor material to the diode series resistance R_d can be determined from a simple model. R_d can be separated into two parts, as follows:

$$R_d = R_c + R_m \qquad (7)$$

Where: R_c is the contribution of the contact resistances and R_m is the contribution of the semiconductor material. The following expression for R_m can be obtained from Fig. 3:

$$R_m = \frac{\rho_p}{\pi r_m^2}\, x_j + \frac{\rho_n}{\pi r_m^2}\, x_n + \int_0^{x_n} \frac{\rho_n}{A}\, dx \qquad (8)$$

The first term in this expression represents the p-region part of the mesa, the second the n-type part of the mesa, and the last the spreading resistance. Because of the impurity diffusion conditions the resistivity ρ_p is usually very small; the resistivity ρ_n is dictated in part by the breakdown voltage required.

Fig. 3 shows several curves of R_m as a function of mesa radius r_m for several sets of parameters. The mesa area is the dominant factor in the expression for R_m when the resistivities on both sides of the junction are small; therefore, R_m rises sharply for small mesa radius. When the resistivity on either side of the junction is high, however, R_m is insensitive to mesa radius.

Values of contact resistance are usually quite small in germanium and silicon devices, but not in GaAs units. In the varactor diode shown in Fig. 1, the contribution R_m is usually less than R_c. Experimental data show that R_c is usually of the order of 0.5 ohm when measured under DC conditions. Contact resistance is not negligible, therefore, although it is not the dominant factor in the diode series resistance.

For junction penetrations of 0.2 to 0.3 mil, it has been experimentally determined that the R_dC product is minimized for values of capacitance

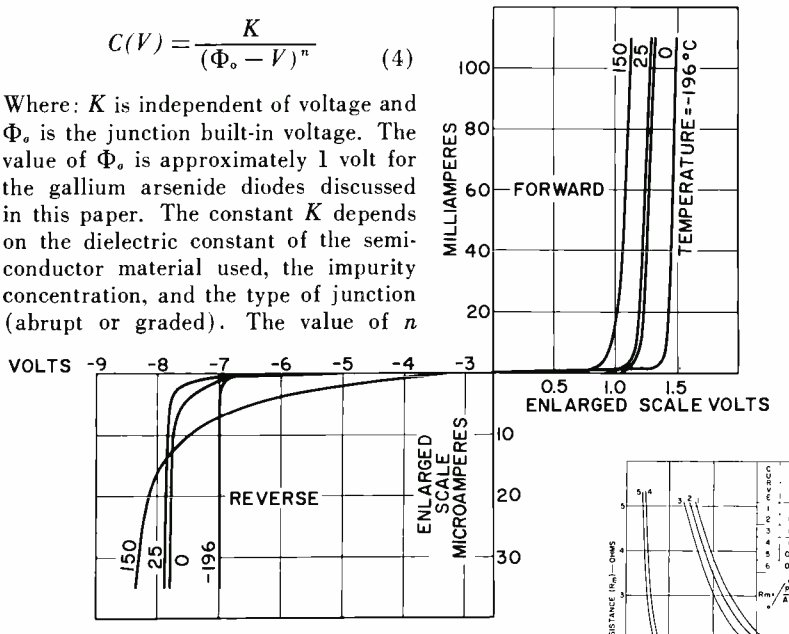

Fig. 4—V-I characteristics.

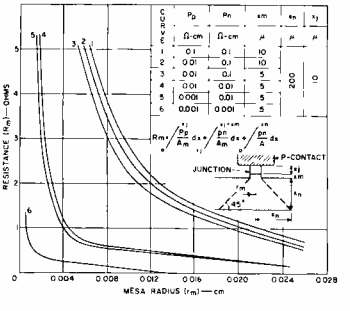

Fig. 3—R_m vs. mesa radius.

Fig. 5—Junction capacitance vs. voltage. Solid: usual n values for GaAs varactor diodes. Dashed: extreme cases for abrupt and graded junctions.

TABLE I—Calculated Values Fractional Change of Junction Capacitance of GaAs Diodes for Abrupt and Graded Junctions.

$\Delta C/C$	Φ_o=0.9 v	Φ_o=1.0 v	Φ_o=1.1 v
Abrupt	0.475	0.466	0.456
Graded	0.350	0.342	0.334

TABLE II—Measurements of GaAs Varactor Diodes

Diode	V_B v @ 10μa	C pf	$\Delta C/C$ fig. of merit	R_S ohms	f_{co} Gc	f^*_{co} Gc
† At 2 Gc, -6v:						
1	12.1	0.260	0.48	1.48	>250	414
2	10.8	0.295	0.42	1.21	>250	445
3	10.4	0.315	0.39	0.93	>250	546
4	9.9	0.249	0.41	1.75	>250	366
At 10 Gc, -6v:						
5	10.0	0.30	0.39	3.12	170	—
6	10.0	0.24	0.37	3.35	198	—
7	11.6	0.35	0.42	2.22	170	—
8	13.4	0.28	0.5	0.64	893	—
9	11.8	0.24	0.36	1.92	346	—

* Actual measured
† Capacitance values @ 1 Mc

TABLE III—Performance of GaAs Varactor Diodes

Signal Frequency, Gc	9.375	8.7
Pump Frequency, Gc	35.8	35.0
Gain, db	15	10
Bandwidth, Mc	16.0	200
Noise Figure, db	2.8*	2.9
Pump Power, mw	125	180

* Includes 2-db circulator loss.

less than 1 pf. In most applications above 1 Gc, the impedance level in microwave systems also requires capacitance values less than 1 pf. The GaAs varactor diodes described in this paper have capacitance values ranging from 0.1 to 1.0 pf. The highest-Q diodes employing the most up-to-date geometry usually exhibit values of 0.3 pf or less.

The magnitude of the negative conductance G_t is also proportional to the capacitance-voltage sensitivity dC/dV. Eq. 6 can be rewritten: (9)

$$G_t = -\omega_t C\left[\frac{1}{2}\frac{V_p}{C}\frac{dC}{dV} - \frac{1}{Q_t}\right]$$

In this equation, the important parameter showing the fractional change of capacitance with respect to voltage is obtained from Eq. 4:

$$\frac{1}{C}\frac{dC}{dV} = \frac{n}{\Phi_o - V} \qquad (10)$$

Thus the capacitance-voltage sensitivity is proportional to the exponent n. As mentioned previously, the value of n is ½ for an abrupt junction and ⅓ for a graded junction. For the junction used in the GaAs varactor diodes, in which the impurity concentration is neither abrupt nor graded, n lies between ½ and ⅓.

A compromise must be made in varactor diodes between the series resistance R_d and the breakdown voltage V_b (voltage at which the leakage current is 10 μa). Although lower concentrations and/or diffusion times result in greater breakdown voltages, they also increase the series resistance. The minimum breakdown voltage required to accommodate 200 mw of pump power at 35 Gc for an X-band parametric amplifier is 6 volts. Breakdown voltages as high as 40 volts have been achieved with the design described, with cutoff frequencies of about 200 Gc at −1 volt.

EXPERIMENTAL RESULTS

Fig. 4 shows the voltage-current characteristics of typical GaAs arsenide varactor diodes at four temperatures ranging from 150 to −196°C. The variation of breakdown voltage at either temperature extreme is less than 15 percent of the value at 25°C. Reverse leakage current is less than 10^{-7} ampere for reverse voltages below the breakdown value for temperatures of 100°C or less. The breakdown characteristic is sharp except at temperatures approaching 150°C. The knee of the forward characteristic becomes sharper with decreasing temperature; this effect is caused by an increase in the junction built-in voltage as the temperature is reduced.

Fig. 5 shows the junction capacitance vs. voltage for typical diodes. The magnitude of the slope of each curve is proportional to the exponent n; larger slopes result in greater capacitance-voltage sensitivity. It can be seen that the slope of the solid curves is superior to that of graded junctions, and approaches that of abrupt junctions.

The slope of the capacitance curve is also dependent to some extent on the value of Φ_o, although little effect was noted in Table I in the voltage range from 0.9 to 1.1 volt. Data are usually plotted for several values of Φ_o, and the value which provides the best straight line is taken as the junction built-in potential. This value is usually about 1.0 volt for GaAs devices. The experimental values measured for n indicate that the impurity profile lies between the abrupt and erfc profiles.

In the early stages of the development program, cutoff frequency was measured at 2 Gc using a slotted-line technique. With this equipment, however, values above 250 Gc are not accurate. Table II shows data for several diodes measured at 2 Gc and −6 volts (diodes 1-4). Actual measured cutoff frequencies are shown (f_{co}*). For diodes 1-4, junction capacitance values (measured at 1 Mc) were less than 0.32 pf, and values of total series resistance were less than 1.75 ohms; also, because the dissipative resistance of the package is less than several tenths of an ohm, the package microwave losses are not large.

Table II also shows measurements made on several GaAs varactor diodes (diodes 5-9) at 10 Gc and −6 volts. The dissipative resistances shown in the table represent total diode and package resistance. No satisfactory method is available for determining separate resistance values at 10 Gc.

Table III shows typical results obtained when these GaAs varactor diodes were used in X-band nondegenerate negative-resistance parametric amplifiers. The cutoff frequency of the diodes was high enough to permit the use of a pump frequency of 35 Gc. In addition, the capacitance-voltage sensitivity of the diodes permitted the use of a relatively low pump power level to achieve adequate gain. The capacitance-voltage sensitivity is also reflected to some extent in the low noise figures. If the sensitivity were too low to achieve gain, the pump power would have to be increased, thus increasing noise.

As shown in Table III, a larger bandwidth can be used if less gain can be tolerated. This exchange of characteristics is possible because the parasitic capacitance and inductance values of the package are quite low.

CONCLUSIONS

It has been shown that very-high-cutoff-frequency diodes may be fabricated from GaAs. Typical values exceed 250 Gc and are significantly higher than values reported in the literature. The V-I characteristic indicates little change in the temperature range from −196 to approximately 100°C. Cutoff frequency and the capacitance-voltage sensitivity are adequate figures of merit to guide design considerations for use of varactors in parametric amplifiers. The circuit-performance gain, bandwidth, and noise figure are outstanding.

ACKNOWLEDGMENT

The authors are pleased to acknowledge the permission of A. Solomon to publish the data in the first column and of R. J. Kampf and V. D. Holaday to publish the data in the second column in Table III, and of H. C. Lee to publish the data in Table II for diodes 5-9.

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New Motives for Microminiaturization ... ECONOMY AND RELIABILITY

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AN OBVIOUS REASON for microminiature circuit packages exists where size and weight are critical, as in aerospace equipment. However, such hardware represents only a portion of electronic products, and size alone can be relatively uncritical in the rest. As new microminiature techniques have developed, another strong motivation has emerged: *a payoff in systems cost reduction and increased reliability.*

To evaluate this payoff, SurfCom made a quantitative analysis using conventional components vs. the Signal Corps-RCA micromodule to represent microminiature techniques. Common estimating parameters (Table I) were developed by averaging fabrication costs and failure rates of commercial and military data-processing equipment at RCA and other companies. All costs were based on average data taken from equipment conforming to good design practice. Similar techniques were used in all packaging to give a common measure for comparison, so that "apples were compared with apples."

TABLE I—Cost and Reliability Estimating Rules

Item	*Time Min:Sec*	*Reliability %/1000 hrs.*	*Cost**
Wire installed in nest or drawer			
Point-to-Point:			
Solder termination	2:20		0.20
Crimp termination	1:30		0.15
Wrap termination	1:20		0.12
Cabled:			
Solder termination	3:00		0.27
Crimp termination	2:10		0.20
Wrap termination	2:00		0.18
Wire installed in cabinet			
Point-to-Point:			
Solder termination	4:00		0.36
Crimp termination	3:10		0.30
Wrap termination	3:00		0.27
Cabled:			
Solder termination	8:00		0.72
Crimp termination	7:00		0.62
Screw terminal	7:00		0.63
Wire installed cabinet to cabinet			
Cabled:			
Solder termination	12:00		1.08
Crimp termination	10:00		0.90
Screw terminal	10:00		0.90
Hole on printed circuit card			0.06
Solder joint on card		0.00023	0.01
Solder joint on terminal		0.0008	0.08
Wire wrap to post		0.00004	0.08
Connector contact pressure type		0.01	0.10
Connector contact screw terminal		0.001	0.08
Crimp contact — wire to termination		0.001	0.08

* Estimating rate: $5.00/hr; ($.09/min)

METHOD

Five package formats, defined by type of plug-in package, were selected (Fig. 1–5) to represent a spectrum of packaging densities that typify solutions to existing packaging problems; their spread in component density was useful for this study. Each design was broken down into natural levels of *circuit, plug-in-board, function,* and *cabinet.* The equipment interconnection cost was calculated from:

$$\frac{\textit{labor \$} + \textit{material \$}}{\textit{(total no. of circuits or micromodules)}}$$

The costs above exclude the cost of the circuit components or micromodules themselves.

The interconnection failure rate per module, which excludes interconnection failures internal to a circuit or micromodule is:

$$\frac{\textit{(\% interconnection failures)/1000 hrs.}}{\textit{(total no. of micromodules or circuits)}}$$

The computations were made by breaking down each subassembly level into its type of board, type and number of connectors, and type of wire and terminations, and then deriving their cost and reliability from Table I. Typical hardware costs (drawers, cabinets, etc.) were added. The over-all results are summarized in Table II.

The use of other estimating rules had very little effect on the final results; proportional differences between packaging techniques remained about the same. Engineering costs can vary from 1/3 to 5 times direct-labor and overhead costs, and because of this wide variance between companies and projects, were not included. To compare *total* costs, engineering and supervision costs should be added for the specific situation involved.

CONCLUSIONS

Per-circuit interconnection costs are lower for the micromodule formats than for the conventional formats, because micromodule support costs are amortized over a large number of circuits. Another miniaturized-package advantage is that long wiring runs (usually twisted-pair or coaxial) and expensive input-output connectors on cabinets are both minimized. *Costs are lowest for the packaging mode that places the most circuits in the plug-in-board level.* Cabinet-to-cabinet wiring is very costly and is considerably reduced or even eliminated with such miniaturized packaging.

In reliability, the variation in the total number of separable connectors is the major factor behind the variation in reliability between the packaging modes. Here again, the *more circuits in the plug-in-board level, the better the reliability figure.*

It can be concluded—assuming like cost and reliability of conventional circuits or miniaturized circuit packages—that the higher the packaging density the lower the cost and failure rate. Fig. 6 relates cost and failure rate vs. system packaging density—*the quantitative answer to the payoff.* If a given organization lacked prior experience with these packaging techniques (SurfCom *had* such experience) then costs would be higher initially ("learning time"); costs shown herein assume such know-how.

Cost and reliability of the RCA micromodules themselves are expected to be somewhat better than component-on-card techniques by 1964. Various types of miniature circuit packages (e.g. micromodules and minimodules) are now in limited production by many companies, and their cost should be competitive with *any conventional-circuit techniques* by 1965. Fig. 7 shows equipment costs per circuit vs. packaging density predicted through 1965, obtained by adding projected costs of microminiature circuit packages to the interconnection costs (engineering costs excluded). More-sophisticated techniques such as integrated circuits, thin-films, etc. should reach cost and reliability levels equal to present technology in 5 to 10 years[1]—which will extend the density shown on Fig. 7 and further reduce cost.

In summary, competition to produce *more equipment per dollar* will force the adoption of minimodules, micromodules, integrated circuits, etc. as fast as these package-circuit techniques become available.

* Work done while author was Administrator, Product Assurance, Digital Communications, SurfCom.

ACKNOWLEDGEMENT

H. K. Sauer and F. D. Cavalier assisted with preparation of the data herein.

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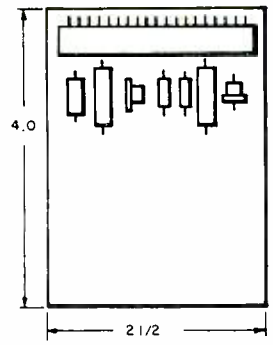

Fig. 1—Conventional-component printed-circuit cards typical of digital equipment. Average density assumed as 72 components (18 components per circuit, 4 circuits per card). Connector pin count sufficient to make this a universal-logic package.

NOTES

Micromodules assumed as averaging a number of wafers equivalent to 18 components each.

Micromodule "plug-in-level" packages (Figs. 2—5) consist of two mounting boards, each holding half the micromodules, which then intermesh to form a booklet. The booklets are interconnected to form "function levels," and these are interconnected in racks to form the "cabinet level."

A "universal-logic" package is one in which input-output and power leads of each circuit are brought out and interconnected at the package connector terminal.

A "logic-on-card" package is one where logic circuit interconnections are on the printed-circuit board.

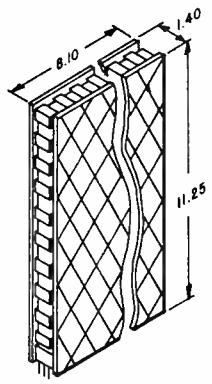

Fig. 2—Universal-logic package of 460 micromodules in wire-wrapped mounting boards.

TABLE II—Interconnection Cost and Reliability vs. Packaging Technique

Refer to illustrations of the plug-in level, Figs. 1–5.

Packaging Technique (Fig. No.)	*Interconnection Costs (Normalized to $ per circuit)*				*Interconnection Failure Rate (Normalized to % per 1000 hrs per module)*				*Parts per Cabinet**
	Plug-in Level	*Function Level*	*Cabinet Level*	*TOTAL*	*Plug-in Level*	*Function Level*	*Cabinet Level*	*TOTAL*	
1	4.08	2.05	0.30	$6.43	0.20	0.02	0.001	0.22%	6,000
2	1.70	0.05	0.02	$1.77	0.13	0.0002	0.00001	0.13%	95,000
3	1.09	0.38	0.03	$1.50	0.08	0.008	0.0001	0.09%	68,000
4	0.45	0.06	0.01	$0.52	0.01	0.001	0.00004	0.01%	146,000
5	0.56	0.17	0.02	$0.75	0.02	0.003	0.001	0.02%	104,000

* *Parts* indicates total number of conventional components or micromodule wafers. In calculating the cabinet-level density, space allotment was made for the memory, power supply, and cooling fans typical for digital equipment. Cabinet dimensions assumed as 2′ x 2′ x 6′ over-all.

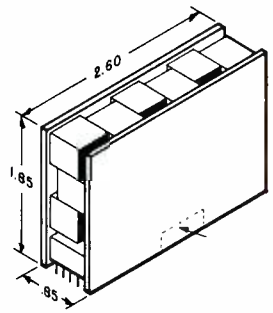

Fig. 3 — Universal-logic package of 16 micromodules in mounting boards.

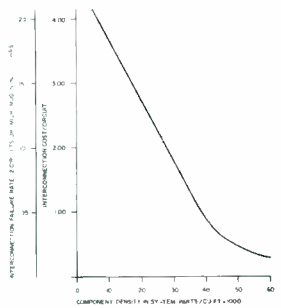

Fig. 6—Effect of component density on cost and failure rate.

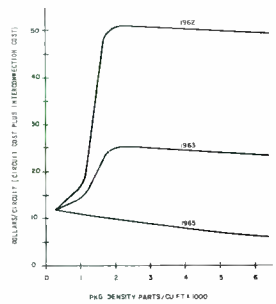

Fig. 7—Equipment cost per circuit vs. packaging density.

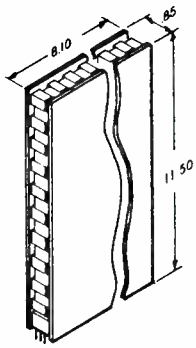

Fig. 4—Logic-on-card package of 460 micromodules in interconnecting printed-circuit boards.

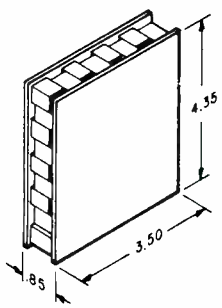

Fig. 5—Logic-on-card package of 64 micromodules in interconnecting printed-circuit boards.

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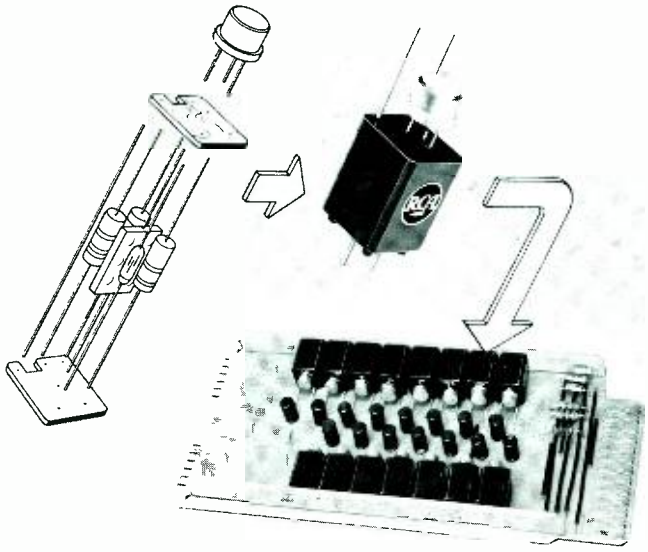

Fig. 1—(clockwise) Principle of the ComLogNet-type minimodule; a minimodule about actual size; and a grouping of minimodules on a ComLogNet board.

A NEW RCA MINIMODULE

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THE RCA minimodules are assemblies of conventional components encapsulated into a package circuit; groupings of minimodules, along with other components, are normally then assembled on a printed-circuit board (Fig. 1). The minimodule is thus one step beyond the conventional printed-circuit-board approach that uses components individually assembled to the board.

Because the minimodule is a tested, reliable package ready for assembly, the equipment builder avoids stocking and handling many individual components, and hardware fabrication is simpler and more economical — especially where many repetitions of one circuit occur. Yet, over-all equipment costs are about the same as for conventional-component-and-board designs.

USE IN ComLogNet

As an example, a new minimodule series (Fig. 1) has been designed for ComLogNet digital equipment. The size of the minimodule was standardized as the volume required to package an inverter (Fig. 2), since 40 percent of the circuits in the ComLogNet computer are inverters varying only in the component value or type. Over-all height of the minimodule inverter (Fig. 1) is 0.8 inch; a transistor extends approximately 0.2 inch above the 0.55-by-0.66-inch base. These dimensions provide optimum volumetric efficiency because relatively few circuit functions require more than one minimodule, and only a small percentage of the circuit functions do not use the entire minimodule volume. Initially, the transistor was mounted flush to the base, but tests showed that the transistor operated approximately 5°C cooler when spaced away from the module — significantly improving reliability.

All minimodule components meet RCA specifications, and the package has passed environmental testing under MIL-STD-202A, including mechanical shock, vibration, humidity, salt spray, and thermal shock. Ambient operating temperature ranges from 10 to 55°C and storage temperature is from −40 to +75°C. At a pulse-repetition frequency of 250 kc, the rise and fall time of the output pulses is between 70 and 80 nsec, and the turn-off and turn-on delay time is between 60 and 70 nsec. Logic levels are ground and 6 volts DC.

FABRICATION

To assemble the ComLogNet minimodule (Fig. 1) the components are threaded into two printed-circuit end boards, clamped, and dip-soldered on each end. Component leads not needed for external connections are cut flush, and the transistor is mounted and soldered. After electrical testing, the completed subassembly is encapsulated in a shell for uniformity, protection, and strength. The end boards, shell, and encapsulant are all fire-retardant, and the epoxy encapsulant includes sufficient filler to provide good heat transfer. Although the temperature rise within the module is only 5 to 8°C at an internal dissipation of 0.5 watt, diodes may be mounted in the subassembly so that they are never adjacent to a high-dissipation resistor.

The minimodule may have leads at one or both ends. The ComLogNet minimodule has power leads at one end, and input-output leads at the other. External leads are spaced at 0.025 inch to conform with the EIA standard grid. Input-output signal leads are at the end opposite from power-supply leads to give isolation, for less pickup and crosstalk, and to facilitate connections to equipment. Power requirements are 6.5 volts DC, 26 volts DC, and −19.5 volts AC.

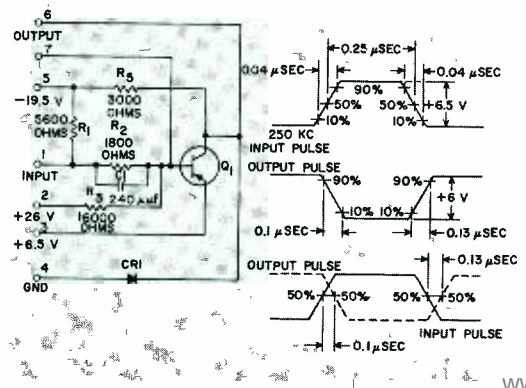
When a group of minimodules are soldered in place on a printed circuit board, power leads are connected to side boards (Fig. 1), and signal leads are soldered into the main board, thus freeing the main board for circuit connections only. In the ComLogNet equipment, air is forced down the center section of the boards to cool the in-facing transistors.

COMMERCIAL MINIMODULES

Some typical minimodules were recently selected from the ComLogNet series and introduced as an RCA product line: an inverter (CPO917), trigger network (CPO918), and power-gate input (CPO919) and output (CPO920), for use in displays and small digital subsystems. Although some custom minimodules also have been designed to ComLogNet packaging specifications, most custom units are designed to meet individual system specifications.

Future plans include a second standard package with twelve exit leads, three on each side, on a 0.150-inch grid spacing—giving a 0.75-inch-square, 0.6-inch-high minimodule. It would be adaptable to a welded assembly, have external leads that could be welded, soldered, or plugged in, and have a low power consumption for high volumetric efficiency.

Fig. 2—Schematic and typical electrical performance of the ComLogNet inverter minimodule.



R. L. WILSON received the BEE from the University of Delaware in 1953, and the MEE from Newark College of Engineering in 1957. He spent six years at Bell Telephone Laboratories on the design, development, and testing of a PCM system. He joined the RCA Semiconductor and Materials Division in 1959 and assumed his present position as Leader, Micromodule Applications, in 1960. His primary responsibility is circuit evaluation, with the goal of adapting micromodules to specific applications. Included is the responsibility for design, development, and testing of commercial modules and of subassemblies or boards containing micromodules. Mr. Wilson has been awarded two patents, and is a Member of IRE and Tau Beta Pi.

DESIGNING MICROMODULES FOR SYSTEM APPLICATIONS

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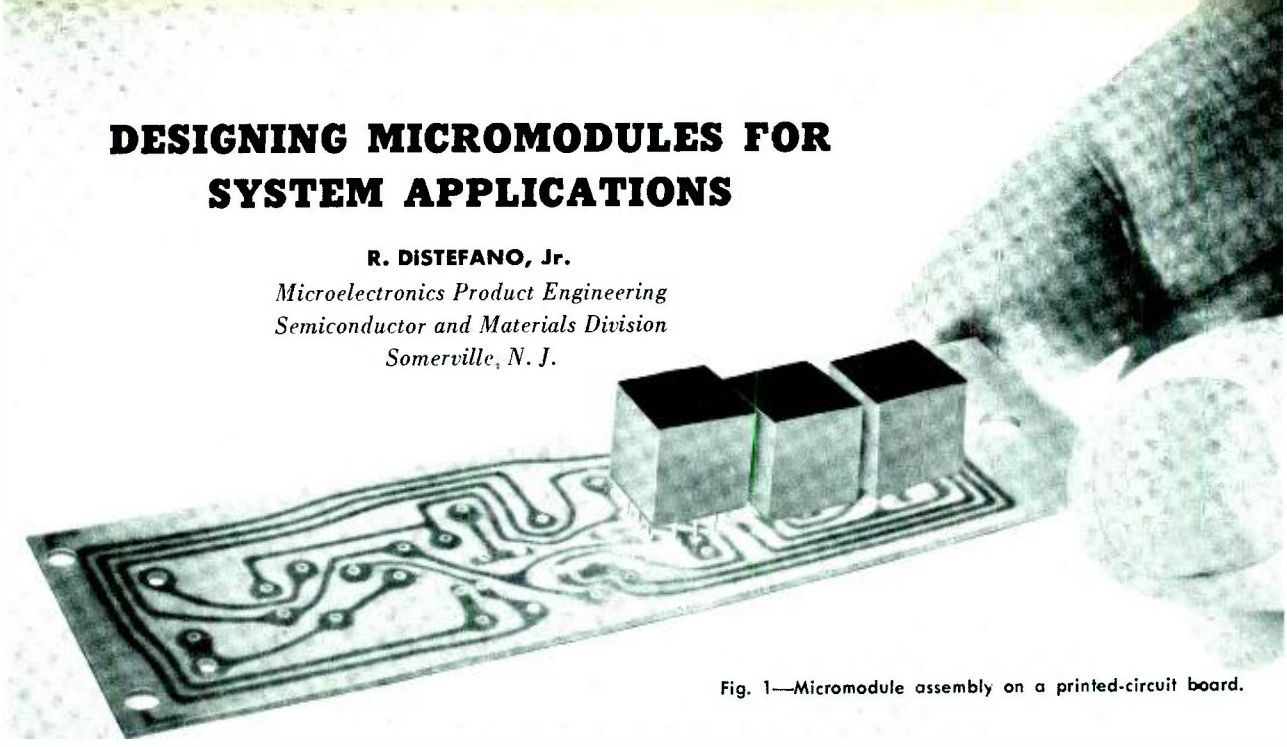

Fig. 1—Micromodule assembly on a printed-circuit board.

The micromodule designer uses these practical methods to make optimum application of micromodules to already-designed circuits as well as to developmental systems. The procedures consider many system parameters—repetitive-circuit economies, packaging requirements, interconnections, relation to non-micromodule components—as well as details of the individual micromodules and their breadboarding.

THERE IS CONTINUING progress in making available, for micromodules, component microelements that offer an ever-larger range of component values and operating specifications. Thus, with more design variables affecting the potential of micromodules in electronic systems, it is important to use practical design procedures that lead to optimum configuration for each micromodule relative to the over-all system.

Up-to-date design methods for micromodules allow their application to existing system designs (with minimum redesign) as well as to development systems that consist only of performance and environmental specifications. In both cases, these design procedures lead to a micromodule breadboard that can be tested against operating and storage-environment requirements.

The micromodule designer, after analyzing the system circuitry, divides it into sections, each representing a potentially separate micromodule. He attempts to minimize the number of different types of micromodules at this time by noting repetitive circuits that can be handled by identical micromodules — especially desirable in systems to be produced in large quantity.

When possible, a micromodule is designed to include a complete function—an amplifier stage, mixer, local oscillator, multivibrator, inverter, or gate. This kind of circuit division provides simplicity and minimizes the number of connections between the micromodules. In certain cases, such as cascaded IF stages, the requirement for isolation of signal leads strongly influences how the circuitry is divided into micromodules.

Although micromodules can be constructed with external leads at both ends, interconnection considerations have made the single-ended micromodule practically mandatory for most systems—normally twelve external leads spaced on a 0.075-inch grid pattern at one end. Interconnection and arrangement in the system is ordinarily done with printed-circuit boards (Fig. 1).

DETERMINING MICROMODULE VOLUME

Although micromodules can be made in heights up to 1 inch, most units are between 0.4 and 0.8 inch high. Micromodule lengths within this range can accommodate many types of stages without exceeding the twelve-lead limit on external connections. Some of the more complicated amplifiers, multivibrators, and other stages are subdivided into two or more micromodules; similarly, some simple, repetitive stages (such as gates) may be combined with one or more similar stages into a single micromodule. In some cases, the maximum height of one or more micromodules in a system is limited by the packaging specifications for the complete system.

To estimate micromodule height, the designer adds up maximum thickness of each wafer, plus 0.010 inch per wafer for the soluble spacers inserted during assembly. (See Table I.)

To this total, an additional 0.120 inch (for the whole micromodule) is added for encapsulation, end wafers, module pedestals, and building tolerance, giving a *design-estimate* height of the micromodule. (The actual height may be as much as 25 percent less, depending upon the actual microelement dimensions.

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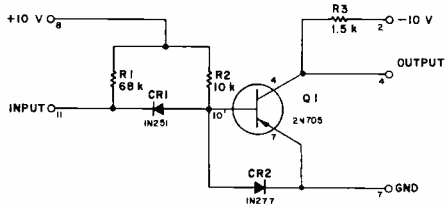

Fig. 2a—A circuit for micromodule implementation.

location or riser-wire cuts, and similar considerations.) With the heights of each micromodule for a system estimated, the system volume or packaging specifications can be checked to determine whether the micromodules must be redesigned or adjusted. Then, detailed design of individual micromodules can begin.

DETAILED MICROMODULE DESIGN

Fig. 2a is an assembly diagram as used by the designer to lay out the circuit of Fig. 2b in micromodule form. Fig. 2a shows the method of numbering riser wires, while Fig. 3 shows the system of numbering notches on the wafers. The rectangular index notch in the corner of the wafer is used for orientation during assembly. On the assembly drawing (Fig. 2a) notch numbers are not shown, but all notches not mounted in the normal (*A1*) position with respect to the riser wires are indicated by three short vertical lines adjacent to the drawing of the far side of the wafer. The position of all wafers not mounted in the normal position is indicated by an arrow pointing to the long side of the wafer index notch, as is the microelement *Q1* (Item 6) in Fig. 2a.

TABLE I

Microelement Space Requirements

Element	*Value Range*	*Space Requirements (Inches)*
* Resistor	—	0.030
Capacitor (T.C.)	to 250 pf	0.030
Capacitor (T.C.)	250 to 1000 pf	0.040
Capacitor (T.C.)	1000 to 2200 pf	0.065
Capacitor (Gen. Purp.)	0.003 to 0.022 μf	0.040
Capacitor (Gen. Purp.)	0.022 to 0.1 μf	0.090
Capacitor, Electrolytic	1 to 3 μf	0.060
Capacitor, Electrolytic	4.7 to 22 μf	0.100
Diode, (Microelement)	—	0.080
Microdiode (Wafer-Mounted)	—	Diode diam. +0.030
Transistor, Microelement	—	0.090
Transistor, TO-46 Package Mounted on Wafer	—	0.115

* Max. dissipation allowance = ½ watt per wafer. Four ⅛-watt or two ¼-watt elements can be accommodated, two or one (respectively) on each side of a wafer. In the case of two resistors on one side, ratio of higher to lower resistance must be < 5, and their terminations arranged so that elements do not cross.

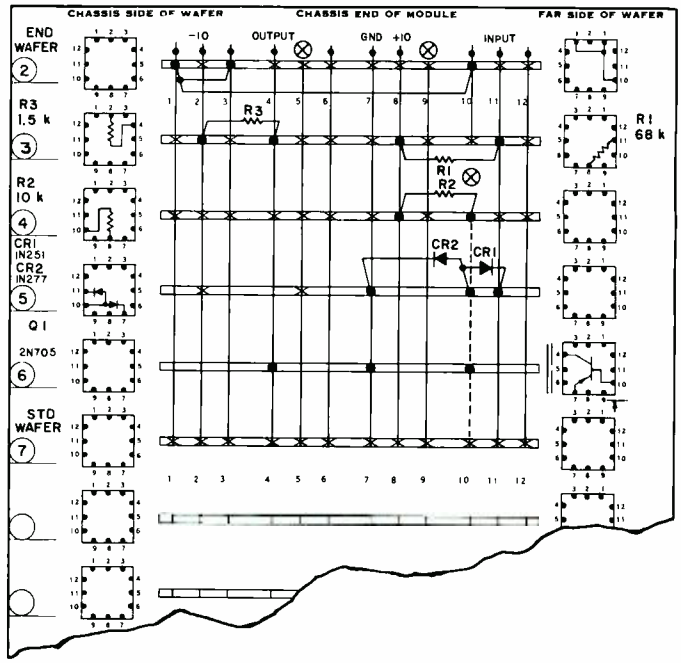

Fig. 2b—Layout of Fig. 2a circuit as a micromodule, using this standard design form.

Riser-Wire Arrangements

The various microelement wafers are connected by hard-drawn, solder-coated copper riser wires, which also form the external leads. These riser wires form the nodes of the external circuitry. If more than twelve nodes are required in one module, one or more of the riser wires is extended only far enough through the module to connect all the elements which meet at one of the nodes. Additional nodes are formed by placing short sections of a riser wire between wafers containing elements to be connected together. This procedure may be repeated with as many as seven additional riser wires to form twenty nodes, but at least one riser wire on each of the four sides of the micromodules must extend along its entire length to form external leads. Where the additional nodes formed by such segmented riser wires consist of connections between adjacent wafers having no more than 0.003 inch of build-up on each side of the substrate, the connection between the wafers is made by "solder-bridging" during the dip-soldering process, and no riser-wire segment is required.

All transistor microelements and mounting wafers for transistors in TO-46 cases are made so that the element is terminated to the wafer notches as shown in Fig. 4 (which also indicates the eight possible mounting positions for a transistor microelement). When a micromodule is designed with two transistors connected in a common-emitter configuration, one can be mounted in the *A1* position and the other in the *B1* position, with a jumper connection located on an end wafer between riser wires *1* and *3*.

An end wafer is usually placed at each end of the micromodule to protect the microelement wafers and provide a mounting for jumpers between riser wires. When necessary, an end wafer may be eliminated if it contains no jumper and if the adjacent wafer does not contain an element on its outer face. Elimination of an end wafer shortens the module height by about 0.015 inch.

Riser wires may also be shortened for additional isolation of a tuned circuit or other critical element located at the end of the module farthest from the chassis. The operation of such circuits may also be improved by locating input and output leads on opposite sides of the micromodule and by designing the module so that the two riser wires on each side of a critical signal lead are grounded on the printed-circuit interconnecting board.

If less than twelve leads are required on a single micromodule for external connections, one or two of the riser wires on each side of the module may be cut off within 0.015 inch of the end wafer after the module is assembled, in order to simplify the wiring on the printed-circuit interconnection board, as in the case of riser wires *5* and *9* in Fig. 2a. However, in all such cases, at least one of the uncut external leads on each of the four module sides must extend through the length of the micro-

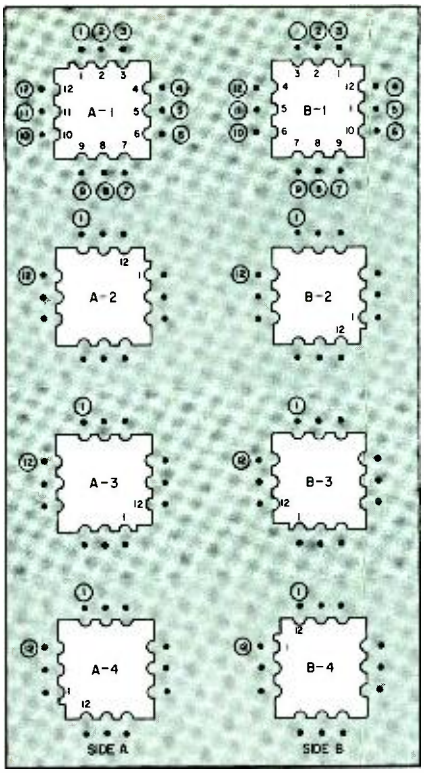

Fig. 3—Eight possible mounting positions for a microelement wafer. (Notch numbers uncircled; corresponding riser-wire numbers circled.)

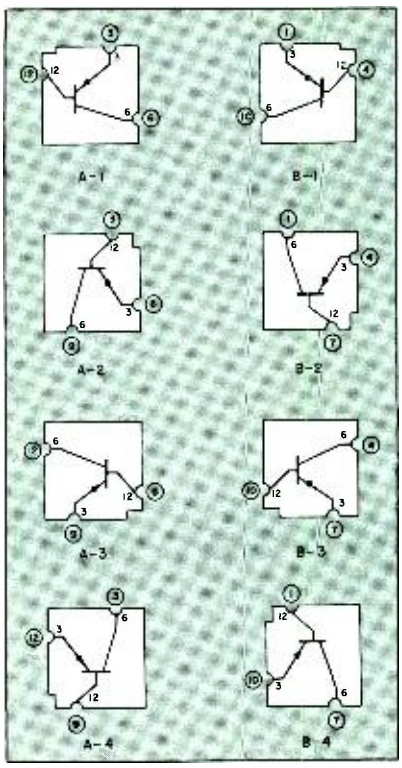

Fig. 4—Eight possible mounting positions for transistor microelement.

module. On occasion, printed-circuit-board interconnection wiring may be further simplified by providing jumpers on micromodule end wafers between leads that do not provide nodes within the micromodule, as shown for the end wafer at the chassis end in Fig. 2a.

Wafer Arrangement

On the basis of these considerations, the designer assigns riser-wire numbers to each of the circuit nodes in a micromodule. When none of the riser wires in a micromodule is shortened and no elements must be isolated from other elements in the micromodule, resistors are usually located at the end closest to the chassis, followed by capacitors, inductors, silicon semiconductors, and germanium semiconductors — in that order, to ensure the most efficient transfer of heat from the micromodule. When one or more of the micromodule riser wires are shortened, the configuration of the various circuit nodes determines the order in which the wafers are assembled. In Fig. 2a, a cut is indicated on riser wire *10* inside the module, and the riser-wire segment used for the node identified as *10′* on Fig. 2b is shown as a dashed line. (In this case, the node cannot be formed by solder bridging because one of the wafers involved has more than 0.003 inch of build-up on both sides.)

Micromodules may be designed to include circuits tuned by trimmer capacitors with ranges up to 16 pf. In such cases, the trimmer is mounted at the end of the module for access when tuning, and the transformer is mounted on the adjacent wafer, which usually includes a larger fixed capacitor connected in parallel with the trimmer. This arrangement also provides some isolation from the remainder of the micromodule.

Breadboarding

In the design of a micromodule system it is often helpful to form a breadboard of the micromodule by mounting hard-drawn wires about 2 inches long in each pin of a twelve-pin phenolic plug. The other ends of the wires are secured to a phenolic disk which is similar to the base in diameter and separated from it by a small 2-inch sleeve mounted at the axis of the connector. The twelve wires are numbered according to the numbers of the plug, and the circuit elements to be used in one micromodule may be connected between the riser wires.

The resulting "totem pole" is an electrical equivalent of the micromodule in analogous physical form. An entire system may be made in this totem-pole configuration, and the test circuitry for the system may be mounted on a master board fitted with receptacles for the totem-pole plugs. This arrangement is often convenient for the tuning, testing, and adjustment of the prototype micromodules or systems of micromodules because, with an adapter socket, one or more micromodules may be substituted for the corresponding totem-pole units.

SYSTEM ASSEMBLY

After the actual micromodules are constructed, they are tested, encapsulated in epoxy resin, and then retested for specification performance. The micromodules are then ready for assembly in the system for which they have been designed (Fig. 1).

The printed-circuit board is designed so that the micromodules are spaced 0.40 inch between centers, but if room is available, this spacing may be increased to accommodate a complex printed-circuit-board wiring pattern on a single side of the printed-circuit board. If spacing between the micromodules cannot be increased beyond 0.40 inch, a double-sided printed-circuit board may be used. A micromodule may be enclosed in a shield covering all surfaces except the chassis end; the major part of the chassis end may be shielded by a portion of the ground plane on the printed-circuit board.

If the system being designed requires circuit elements that have not yet been adapted to the micromodule form, the conventional components may be mounted directly on the printed-circuit board near the micromodules.

SUMMARY

The foregoing is a general survey of micromodule system design procedure as it exists in December 1961. As a result of extensive development work underway at the time of writing, the near future will further improve on the already large range of component values and operating specifications of microelements now available. It is also anticipated that the constantly improving, very favorable micromodule operating reliability will become an achievement goal for all future generations of microelectronic concepts.

ACKNOWLEDGEMENT

The guidance and comments offered by the author's colleagues, particularly by A. N. Gardiner, W. Oates, D. Stubbins, B. Vonderschmitt, R. Wilson, and R. Samuel are gratefully acknowledged.

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HIGH-SPEED TUNNEL-DIODE LOGIC CIRCUITS

A compatible set of tunnel-diode logic circuits with 1-nsec logic delays and 200-Mc repetition rates has been developed. Directionality is obtained with low-peak-current tunnel diodes called tunnel rectifiers, and gain is provided by monostable pulse amplifiers. For storage registers, a level-producing bistable circuit is employed. Timing problems caused by the increased effect of wiring delays at these speeds have been reduced by the provision of gating levels against pulses wherever necessary.

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HANOCH UR, who was born in Bucharest, Romania, received the BS and Dipl. Ing. degrees from the Technion-Israel Institute of Technology, Haifa, in 1954 and 1955, respectively. From 1955 to 1956, he was a research assistant at the Computing Laboratory of Purdue University, Lafayette, Ind., and received the MSEE from Purdue in 1956. After a short period as a logical designer with Univac, St. Paul, Minn., he joined the Polytechnic Institute of Brooklyn, Brooklyn, N. Y. as an instructor. He joined RCA-EDP in 1959 where he has been working on tunnel-diode applications for high-speed computers. Mr. Ur is a member of Sigma Xi and the Institute of Radio Engineers.

R. H. BERGMAN received his BSEE from Rutgers University, New Brunswick, New Jersey, in 1953. He joined RCA in 1953, where he has worked primarily on pulse and digital circuitry, analog-to-digital conversion, ultrasonic measurements, and the application of tunnel diodes to computers. He served in the U. S. Signal Corps from 1954 to 1956 and returned to RCA the same year. Late in 1960, Mr. Bergman was promoted to his present position of Leader, Design and Development Engineering, where he is responsible for logic-circuit work on a development project for a 1-gigacycle computer. Mr. Bergman is a member of the Institute of Radio Engineers, Tau Beta Pi, and Eta Kappa Nu.

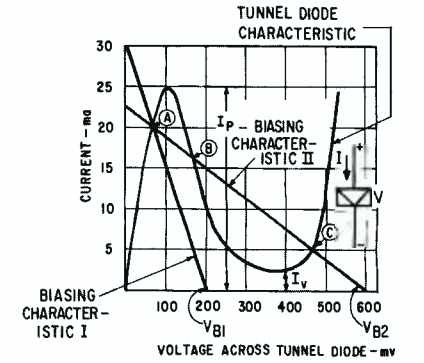


Fig. 1a—Two modes of operation for a tunnel diode.

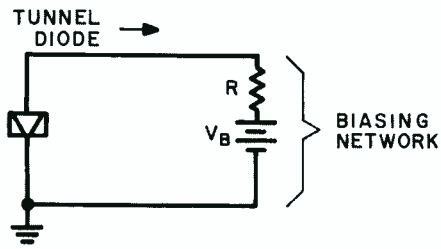


Fig. 1b—Tunnel-diode circuit.

THE TUNNEL DIODE, a high-frequency, low-power device exhibiting negative resistance, can be used to obtain fast switching and high-frequency amplification.[1-4] Since it is also compact, simple, and rugged in construction, it is especially promising for high-speed digital-computer applications, where operating speed, reliability, size, and low power consumption are of the utmost importance.[2,3,5,6]

A typical tunnel-diode characteristic (Fig. 1a) exhibits a voltage-controlled negative resistance; with appropriate biasing, this device may be used in a monostable or bistable mode.[1,2,3] A circuit for obtaining these modes of operation is shown in Fig. 1b. This circuit provides the biasing characteristics shown in Fig. 1a. Biasing characteristic *I* provides one stable operating point *A*, while biasing characteristic *II* provides two stable operating points *A* and *C*. The intersection at *B* is unstable. The tunnel diode *monostable* circuit provides a practical way of obtaining amplification and performing logic functions; the *bistable* circuit provides storage.

MONOSTABLE CIRCUITS

The following analysis considers a simple monostable circuit (Fig. 2a) and a linear biasing characteristic (Fig. 2b); however, this method of analysis also applies for nonlinear biasing character-

istics which, as will be shown later, are more desirable. This method has been employed quite successfully to study the transient behavior of nonlinear circuits of much greater complexity.

General Transient Analysis

In Fig. 2a, R and V_B form the biasing characteristic which intersects the tunnel-diode characteristic at *1* in Fig. 2b. To simplify analysis, assume that the inductance L of Fig. 2a is relatively large so that there is negligible change of current in R as the diode switches from *1* to *3* (Fig. 2b). Under these conditions, if a current step input is forced into node *1* of Fig. 2a, it all goes into the tunnel diode. When the total current into the tunnel diode exceeds the tunnel-diode peak current, the operating point switches to *3* along the trajectory indicated by the dotted lines (Fig. 2b). (The trajectory is a plot of the total current available to the tunnel diode versus the voltage across the tunnel diode.) Thus, while the diode switches from *1* to *3*, the available current is $I_{in} + I_B$, resulting in a constant-current dynamic load line of this magnitude.

The speed of switching from *1* to *3* depends on how quickly the diode capacitor C can be charged to the new voltage. In general, the instantaneous rate of change in voltage across a capacitor C may be expressed as:

$$\frac{dv}{dt} = \frac{i_c}{C} \qquad (1)$$

Where: v = capacitor voltage, i_c = the charging current, and t = time. In this case, i_c is the difference between the total available current, $I_B + I_{in}$, and diode current, i_d. Instantaneous charging current i_c is the distance KL. Thus, for a given diode, the larger KL, the faster switching takes place.

If immediately after reaching point *3*, the input is removed, the operating point of the tunnel diode moves to 4. This, however, is not a stable state, and the current in L decays, causing the dynamic operating point to proceed toward *5*. (If the biasing characteristic *II* of Fig. 1a had been used, there would be a stable intersection somewhere between *4* and *5*, a static operating point where the diode would remain indefinitely. This represents a storage of information and is the property underlying the bistable circuit to be described later.) The speed of moving from *4* to *5* depends upon how quickly the current in the inductance can change. In general, the instantaneous rate of change of current in inductance L may be expressed as:

$$\frac{di}{dt} = \frac{v_L}{L} \qquad (2)$$

Where: i = current in the inductance, v_L = voltage across the inductance, and t = time. In this case, v_L is the difference between the biasing network voltage v_r and the tunnel-diode voltage v_d (Fig. 2a). In Fig. 2b, v_L is the distance PM. Thus for a given inductance, the larger the distance PM, the faster the dynamic operating point moves (relaxes) from *4* to *5*. When *5* is reached, the current in L continues decreasing, since v_L is not zero. This action takes the diode once again into the negative-resistance region, causing it to switch to *6* by a similar mechanism that caused it to switch from *1* to *3*.

Point *6* is still not stable, since v_L is not zero. Note, however, that v_L has changed sign, which causes the current in L to increase until point *1* is reached. Here again, for a given inductance, the larger the distance QN, the faster the operating point moves (relaxes) from *6* to *1*. Point *1*, the initial operating point, is stable, since v_L and i_c equal zero.

Voltage Waveform

The voltage v_d obtained from the switching trajectory of Fig. 2b is shown as a function of time in Fig. 2c, with the waveform of the complete cycle subdivided into intervals. Referring to Figs. 2b and 2c, the delay time is a function of i_c/C in the region *1* to *2*. The magnitude of i_c at the tunnel-diode peak is called the overdrive and is expressed as a percentage of the tunnel-diode peak current I_p. The relationship between total switching time and overdrive is shown in Fig. 3; this curve is valid for the circuit of Fig. 2a. The rise time and fall time are functions of i_c/C in their respective regions; the pulse width and recovery time are a function of v_L/L in their respective regions.

Thus, the monostable circuit provides a reshaped voltage pulse and can supply an output current approximately equal to I_B (Fig. 2b). This output current is several times the magnitude of I_{in}. Thus, current amplification is obtained.

Nonlinear Biasing

For high-speed operation, the total cycle time of Fig. 2c must be reduced to a minimum. Most of this time is made up of the pulse width and recovery period, which can be reduced by reducing the inductance (as explained previously). However, to obtain the operating speed of interest (5-nsec total cycle time for tunnel diodes having

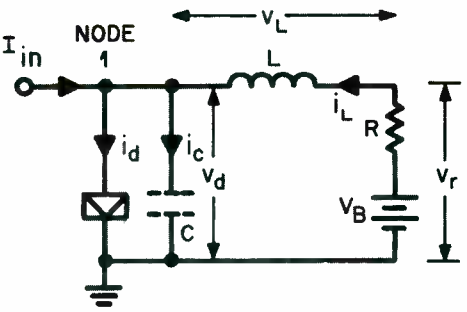


Fig. 2a—Basic monostable circuit.

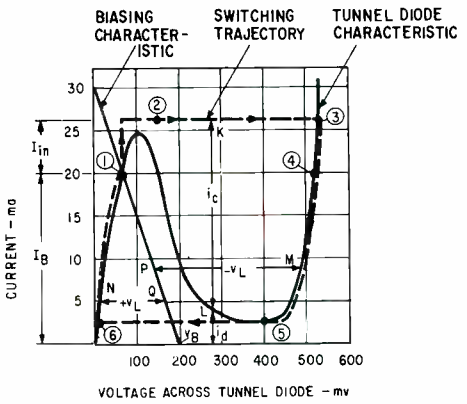


Fig. 2b—Graphical analysis of monostable switching.

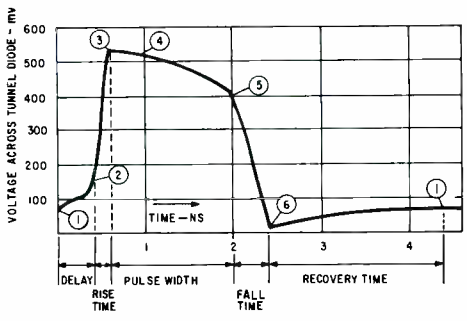


Fig. 2c—Output voltage waveform of monostable circuit.

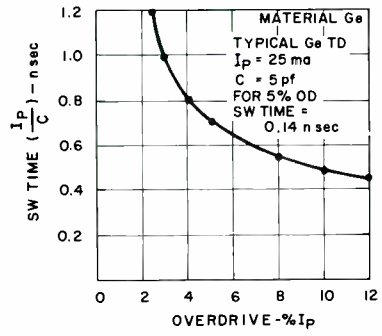


Fig. 3—Normalized switching time vs. overdrive.

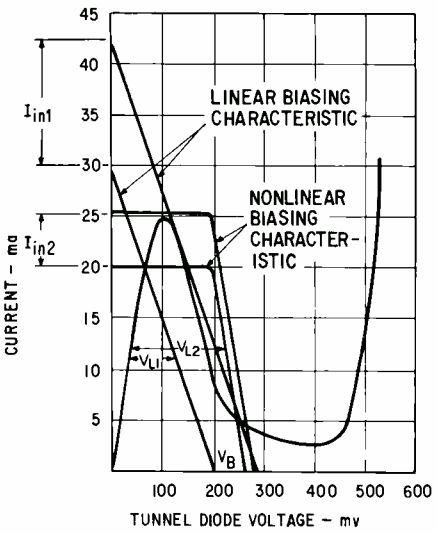


Fig. 4a—Comparison between linear and nonlinear biasing.

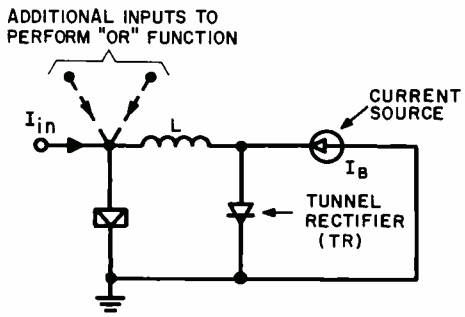


Fig. 4b—Monostable circuit with nonlinear biasing network.

$I_p/C = 5$ ma/pf) the inductance has to be made so small (5 nh) that it no longer blocks I_{in} from flowing into R, as assumed in Fig. 2a. Therefore, I_{in} has to be increased to I_{in_1} (Fig. 4a); this reduces the current amplification, thus reducing the usefulness of this circuit.

This situation is remedied with the nonlinear biasing characteristic of Fig. 4a, which is obtained with the current source I_B and tunnel rectifier TR of Fig. 4b. (The idealized characteristic of a tunnel rectifier is shown in Fig. 5.) In the circuit of Fig. 4b, the tunnel rectifier is nonconductive up to 200 mv, permitting the input current I_{in} to flow into the tunnel diode until it has switched over the peak. After 200 mv is exceeded, the tunnel rectifier conducts, producing a mode of operation similar to Fig. 2b. The relative magnitudes of I_{in} required with linear and nonlinear biasing is indicated in Fig. 4a. The action of the tunnel rectifier in this configuration is referred to as *clamping*.

Nonlinear biasing has thus eliminated the need for any inductance as far as switching over the peak is concerned; however, some inductance is needed to permit an external load to take current before it is absorbed by the clamp. If linear biasing were used, this inductance would still cause a long recovery from points *6* to *1* (Figs. 2b and 2c). However, as explained for Fig. 2b, this recovery time may be reduced by increasing v_{L1} in this region. Here again, the nonlinear biasing offers an advantage, since in this region v_{L2} is considerably larger than with the linear biasing. Thus, a nonlinear biasing network, as shown, provides efficient switching and fast recovery.

Tunnel-Diode Or Gate

The complete circuit of a tunnel-diode *or* gate (Fig. 6) consists of two monostable stages cascaded to provide the required current amplification. A nominal input of 8 ma into either input *1* or *2* causes TD_1 to fire, which in turn fires TD_2 via the coupling rectifier TR_c. The three outputs of TD_2 are each capable of supplying 8 ma to the input of another gate.

Although only two inputs are shown, this gate will function with a maximum of five inputs; however, with two stages, the output is limited to three. The number of outputs (fan out) is primarily limited by the component tolerances. The nominal delay for this circuit is 1.0 nsec, with a 200-Mc repetition rate. A typical output waveform of an *or* gate is shown in Fig. 8.

Tunnel-Diode And Gate

The *or* gate produces an output if any one of the inputs are high. If, however, the bias current of the first stage of Fig. 6 is reduced so that one input is insufficient to switch it—but the sum of the currents of two inputs are sufficiently large to produce switching—the basic property of an *and* gate is obtained (Fig. 7).

One of the *and*-gate inputs is a level obtained from a bistable circuit; the other input is a pulse from an *or* gate or another *and* gate. The use of pulse gating against a level is employed to avoid the timing problems encountered with a pulse gated against a pulse, particularly at gigacycle speeds.

The tolerance requirements for a circuit of this type are more severe than for the *or* gate. Less current is available from the first stage; to overcome this limitation, two additional stages are provided to obtain a fan out of two. The nominal delay for this circuit is 1.2 nsec with a 200-Mc repetition rate.

DC Tolerance Analysis

To determine the gain obtainable from the circuits and specify components and their variation, a worst-case tolerance analysis was performed. In the analysis, variations in power supplies, bias resistors, tunnel diodes, and tunnel rectifiers were considered. Some of the additional conditions were: A guaranteed minimum overdrive when switching of a tunnel diode was desired; a safety factor when switching was not desired; and an allowance for undesired transients when the circuits were interconnected. From the specified variations and the imposed conditions, the number of stages needed to provide required gain or fan out was determined.

BISTABLE CIRCUITS

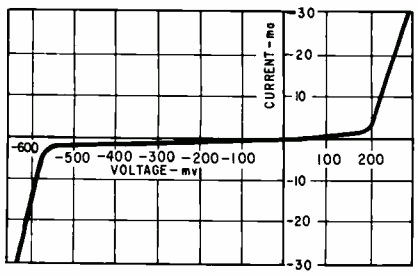
As indicated in Fig. 1a, a tunnel diode with a suitable load line can be operated in a bistable mode. This property is used to obtain storage. The bistable unit and the circuits required for setting and resetting will be described in the following sections.

Principle of Operation

The bistable circuit may be divided into a number of blocks performing various functions (Fig. 9). Only one block on Fig. 9 is bistable; the others are monostable, and their only function is to switch the bistable unit to its high or low state via the available positive-pulse *set* and *reset* inputs. Any one of the set inputs is amplified by the set amplifier which switches the bistable unit to its high-voltage state—representing a logic *1*. Any one of the reset inputs switches the inverter driver, which activates the inverter to produce a negative pulse that switches the bistable unit to its low-voltage state—representing a logic *0*.

To illustrate the operating principle of the bistable circuit, a simplified circuit (Fig. 10) will be considered (with some of the stray reactive elements omitted). The Fig. 10 circuit is divided into parts corresponding to those on the block diagram of Fig. 9.

Fig. 5—Idealized rectifier characteristic.



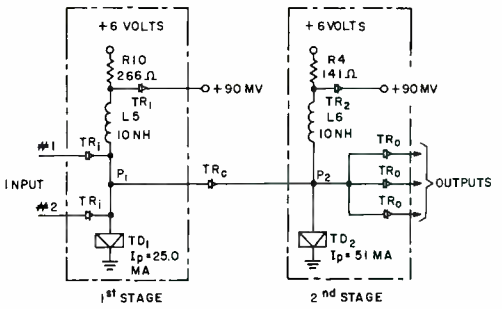


Fig. 6—Tunnel diode OR gate.

Setting

The set amplifier is the tunnel-diode monostable circuit described earlier, designed so that an 8-ma set input is required to initiate switching. The output current of the set amplifier flows through TR_6 into TD_6 of the bistable unit (Fig. 10).

The idealized switching characteristic of the bistable unit (Fig. 11) consists of a tunnel diode intersected by a load line at two stable points A and C. This load line is formed by the combined characteristic of the three *and* gates that TD_6 is driving. Assuming that TD_6 is in the *0* state (point A), the current supplied by the set amplifier causes TD_6 to switch over the peak along the indicated trajectory and stop at point C. The bistable circuit is thus set to its high state.

Resetting

When a positive current pulse is forced into node *9*, TD_1 switches to its high voltage state. This causes the current in TR_1 to increase and the current in TD_1 (I_1) to decrease. A decrease in I_1 acts as a negative current input which triggers the inverter to produce a negative pulse. (The inverter, which consists of TD_3, TR_4, and I_E, is an inverted monostable circuit of the type described in Fig. 4b). The negative pulse causes reverse conduction in TR_5 (characteristic shown in Fig. 5).

The flow of current in TR_5 diverts most of the current from the current source I_D, causing the static loadline of Fig. 11 to move down. When the loadline moves down such that the intersection at C becomes unstable or disappears, TD_6 becomes temporarily unstable and starts switching towards point D along the indicated trajectory. Resetting is completed when the inverter output pulse becomes zero, at which time the operating point returns to point A.

Experimental Complete Bistable Circuit

In the complete bistable circuit (Fig. 12), the choice of circuit components and design was based on DC tolerance calculations and digital-computer simulation.

The set and reset inputs are applied through tunnel rectifiers to isolate the circuit from preceding logic stages. The current sources are connected directly to the rectifiers TR_4 and TR_{11}, instead of to nodes *8* and *11* as was done in the simplified circuit of Fig. 10. The difference between the two is very slight; however, the connection in Fig. 12 is more desirable, since it prevents R_8 and R_{11} from loading the tunnel diodes.

The inductances in series with the output rectifiers on TD_6 are used to obtain more-efficient reset action because during the initial period of resetting, the series inductances prevent the currents in the *and* gates from changing and thus permit more of the reset current to go through TD_6. The addition of inductance, however, increases the time required for establishing a new level in the *and* gate, reducing somewhat the over-all repetition rate.

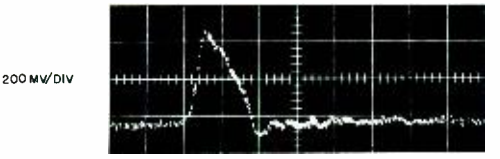


Fig. 8—Photograph of an OR gate output waveform.

An unassembled and an assembled bistable wafer are shown in Fig. 13a. Care was taken in the wafer layout to keep stray reactances to a minimum. The output waveform resulting from a set input followed by a reset input 5 nsec later is shown in Fig. 13b, taken at a point corresponding to node *10* of Fig. 12.

LOGIC CIRCUIT INTERCONNECTION

As the rise times of logic circuits are shortened into the nanosecond region, increased attention must be paid to the methods by which these circuits are

Fig. 9—Block diagram of bistable circuit.

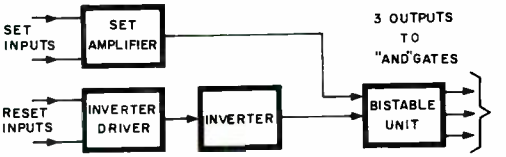


Fig. 7—Tunnel diode AND gate.

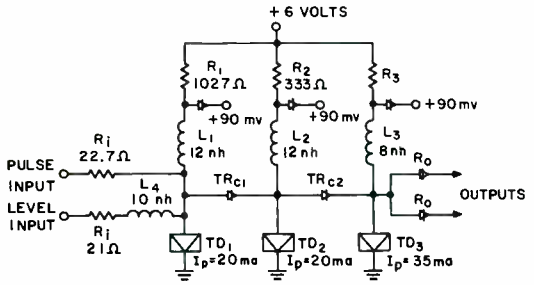
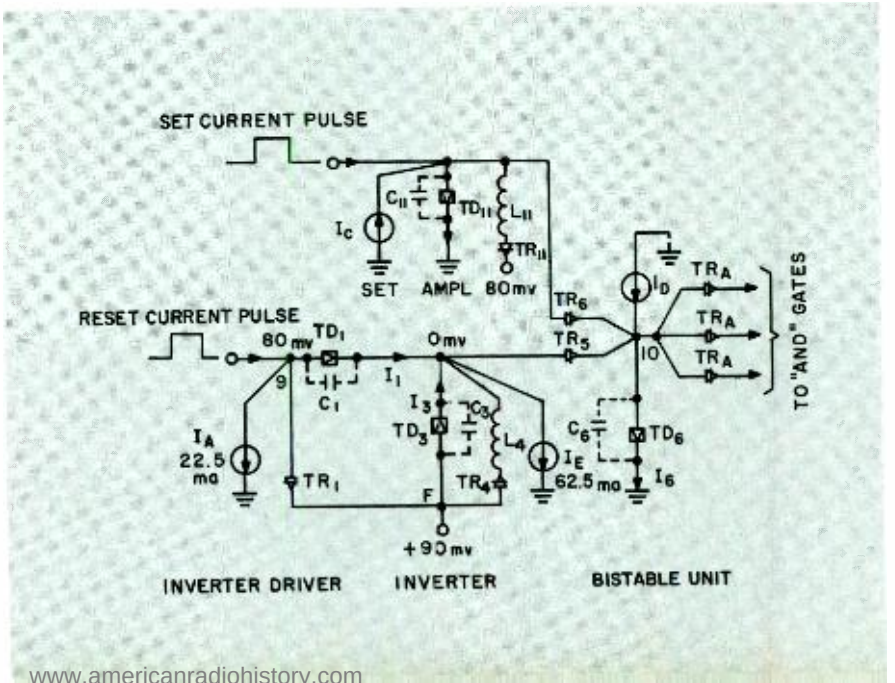


Fig. 10—Simplified diagram of bistable circuit.



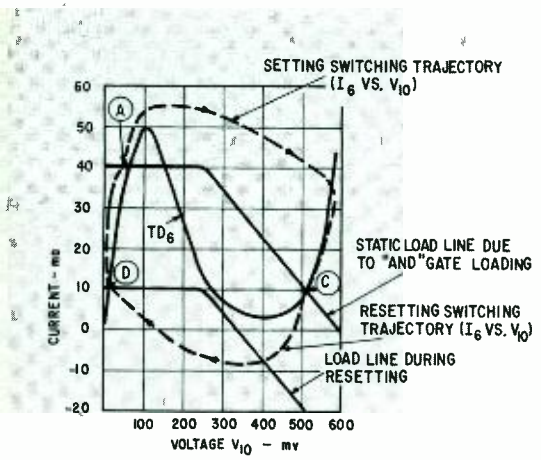


Fig. 11—Idealized switching characteristic of bistable unit.

interconnected. Some of the problems are crosstalk, the effect of common ground paths, and line termination. When the propagation times are long compared to the rise time of the interconnection system, the distributive effect of the interconnection cannot be neglected. Also, as the speed of circuits is increased without an equivalent reduction in their volume, the interconnection delay becomes a greater percentage of the total. At some point, most interconnections will have to be treated as transmission lines. For this reason, it is important to design the interconnection system with greatest efficiency, i.e., use low-dielectric-constant materials for maximum propagation velocity and terminate transmission lines to make efficient use of the transmitted power.

In the case of the circuits described here, typical logic delays are of the order of 1 nsec, with rise times of 0.2 nsec. Fabrication requires typical interconnection lengths of 2 to 6 inches.

It was decided to use a miniature coaxial cable for all logic interconnections. One requirement was that its design be compatible with the circuits with respect to maintaining directionality and required level of input, output, and feedback signals.

ACKNOWLEDGEMENT

The work described here is the product of a joint effort by the Logic Circuit Group of the EDP Advanced Development section. Credit is due the following individuals for their part in this work: L. J. Bazin, for preliminary tolerance analysis; R. Cheuh, for tolerance analysis of the monostable circuits; E. C. Cornish, for tolerance analysis and laboratory development of the bistable circuit; and C. Pendred for simulation of the circuits on the RCA 501 computer.

Some of the basic ideas which lead to the development of the resetting circuit were contributed by M. M. Kaufman.

The authors also wish to express their gratitude to their colleagues at Pennsauken, Somerville and Princeton for their support and cooperation. Particular thanks are due R. K. Lockhart and J. N. Marshall for their guidance and support.

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6. R. K. Lockhart, "Development of a 1000-Mc Computer," RCA Engineer, Vol. 6, No. 4, Dec.-Jan. 1961.

Fig. 13a—Unassembled and assembled bistable wafer.

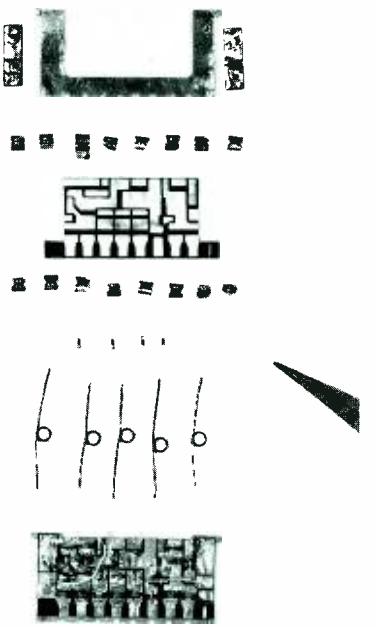


Fig. 12—Schematic diagram of bistable circuit with nominal values.

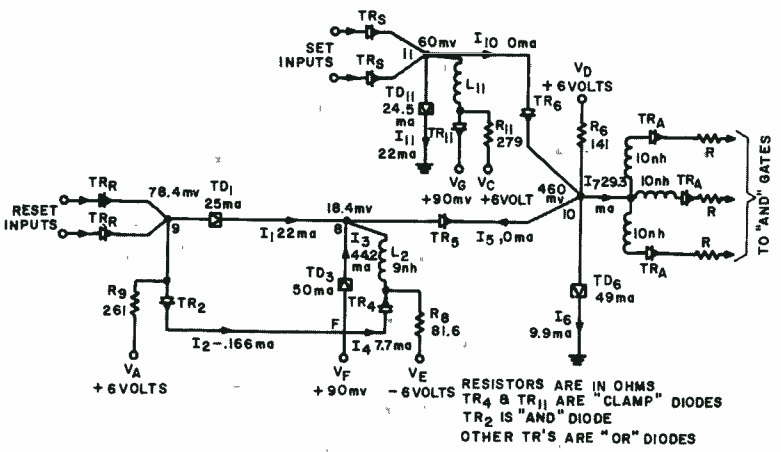
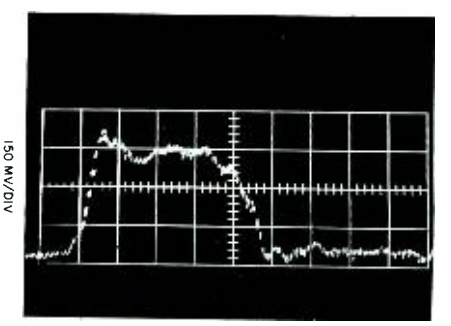


Fig. 13b—Output waveform of bistable circuit.



NEW PRODUCTS

The ETD Approach

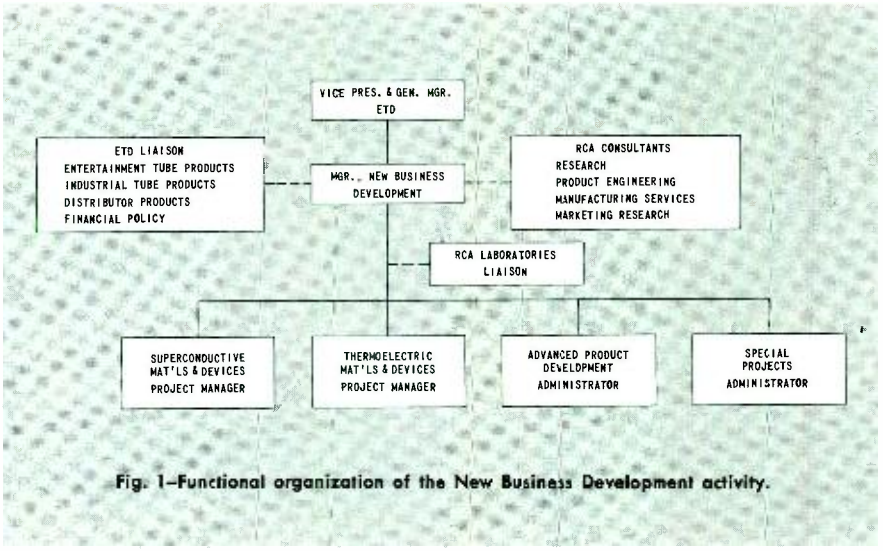


Fig. 1–Functional organization of the New Business Development activity.

Today, there is increasing interest in non-tube products in the Electron Tube Division. To pursue this interest, the ETD New Business Development activity is engaged in long-range planning and liaison with other RCA research and engineering activities to find, analyze, develop, and bring to commercial fruition new product lines of promise.

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Administrator
Advanced Product Development
ETD, Harrison, N. J.

D. W. CHACE
Sr. Tech. Administrator
RCA Laboratories
Princeton, N. J.

THE SIGN OVER the door to the factory building in Harrison, New Jersey, proudly announces, "HOME OF THE WORLD'S BEST TUBE MAKERS." The time is arriving for the addition of a postscript which says, "*We also make superior energy-conversion, superconductive, and other electronic devices.*"

Non-tube products *are not new* to RCA's Electron Tube Division. As an example, ETD developed a substantial engineering, manufacturing, and marketing organization for transistors which became the nucleus of RCA's Semiconductor and Materials Division in December 1955. Although ETD's excellent growth (roughly 100 percent in the last decade) has been largely due to innovation and diversification in electron tubes, there is today new and sharp emphasis on non-tube developments of commercial promise.

WHY NON-TUBE PRODUCTS AT ETD?

Continued technical innovation will sustain the continued growth of major portions of the electron-tube business. There is no known device, for example, that challenges the supremacy of the tube for generating megawatts of power. Yet, solid-state devices have already made inroads into segments of the tube business, and there is every reason to suppose that this trend will continue. At the same time, the continuing technical improvement of tubes themselves is increasing operating life to an extent that significantly diminishes the market for replacements.

Thus, there is increasing interest today in ETD in new products and new business opportunities in such diverse areas as thermoelectric and thermionic power converters, super-conducting materials and magnets, electroluminescent and ferroelectric materials and panels for information displays or special lighting effects, dry-reed switches for use as high-speed relays in both military and commercial data processing systems, high-vacuum vessels for space simulators, and elements for computer memory systems.

The focal point of such interests is the *New Business Development* activity with headquarters in Harrison, N. J.—an activity in many ways unique to RCA.

NEW BUSINESS DEVELOPMENT OBJECTIVES

The New Business activity has the following major objectives aimed at adding new and profitable products to the existing ETD line:

1) to stimulate suggestions for new non-tube product ideas which can profitably exploit the well-developed, wide-range ETD skills;
2) to screen and evaluate such ideas;
3) to formulate programs for the development of promising new products;
4) to evaluate and recommend ETD manpower and facilities suitable for the development of promising new products and to supplement existing manpower and facilities when necessary;
5) to formulate a business plan for the development and commercialization of new products; and
6) to evaluate existing new-product projects on a continuing basis, particularly in relation to the over-all ETD business objectives.

A TOP-LEVEL STAFF AND COMMITTEE OF CORPORATE CONSULTANTS

The permanent staff of the New Business Development activity is relatively small—five men, including the manager, L. R. Day, who reports directly to D. Y. Smith, the Vice-President and General Manager of ETD. Organizationally, therefore, the activity is a top-level staff function within ETD. The activity relies heavily on other talents, however, both within ETD and in other major RCA line and staff activities. This interplay has been largely responsible for a recent swift accumulation of new product ideas, some of which are already the subject of substantial development programs.

The help of individuals familiar with broad segments of RCA's business and product lines was sought in the beginning. A committee of corporate consultants was formed representing re-

search, product engineering, manufacturing, and marketing (Fig. 1). These individuals bring a broad background of RCA experience and know-how to bear on the wide range of problems involved in the evolution of new products. Their familiarity with RCA's corporate objectives and the objectives and programs of all RCA product divisions is particularly significant. Just as important, they are familiar with ETD capabilities. Particularly noteworthy are the backgrounds of D. F. Schmit, Staff Vice President, Product Engineering, as a former Chief Engineer of the Tube Division; and H. W. Leverenz, Associate Director of RCA Laboratories, as a Tube Division research and development engineer prior to the formation of RCA Laboratories.

The New Business activity also relies heavily on the ETD operating departments. Each department has a designated individual who works closely with New Business Development on matters of general interest and assists in organizing specific projects on an individual basis. The experience and, in particular, the working contact of the departmental representatives is an important —indeed vital—ingredient in the program.

Starting in 1962, one master list of new business projects is maintained by New Business Development, and one person is assigned over-all responsibility for each project on the list. A business plan is prepared for each project and funding is then authorized and controlled by the Manager, New Business Development, from a special budget created from ETD funds. At regular intervals, the status of each project and proposed additions or deletions are reviewed with D. Y. Smith and his staff (Fig. 2). By this means, over-all responsibility for new business is viewed primarily from a divisional level and is divorced from the often dissimilar interests of the individual product lines.

LIAISON WITH RCA LABORATORIES

Since its formation, the New Business Development activity has looked to the RCA Laboratories for advice and help, not only in interpreting and evaluating technical trends, but also for specific non-tube research results that might be the subject of ETD development and commercial exploitation. As one means of establishing contact on a daily basis with RCA Laboratories, D. W. Chace [co-author] was assigned by Princeton management to work directly with the New Business Development activity. The close technical and management cooperation between ETD and the RCA

Fig. 2–New product review meeting attended by D. Y. Smith, Vice President and General Manager, Electron Tube Division, and staff. Pictured, starting at lower left and going clockwise are: J. J. Kearny, L. A. Kameen, E. P. Hirsch, T. J. Scanlon, C. E. Burnett, K. G. Bucklin, (standing), J. B. Farese, F. P. Aitelli, D. Y. Smith, M. Kalen, and L. R. Day.

Fig. 3–New thermoelectric material being discussed by (l. to r.) Dr. F. D. Rosi, Associate Laboratory Director, Materials Research Laboratory, RCA Laboratories. U. S. Freedman, Manager, Chemical and Physical Laboratory, and P. P. Roudakoff, Project Manoger, Thermoelectric Materials and Devices.

Fig. 4–Kurt Strater (l.) and Lewis Gnau (r.) of the Harrison Chemical and Physical Laboratory, together with Dr. Joseph J. Hanak, of the RCA Laboratories at Princeton, examining niobium tin superconductive wire being produced by new RCA technique. A wire-wound magnet using this new material weighing only 20 pounds, exclusive of refrigerating equipment, when pulsed by a 6-volt battery is expected to produce a magnetic field over a volume that now requires a 100-ton electromagnet operated continuously from a 100-kw power supply.

WALLACE M. JAMES received the BSEE and a BS in Engineering (a five-year degree) from the University of Kansas in 1925. He held a commission in the U. S. Engineer Reserve from that time until 1934. After graduation, he worked in the Radio Receiver Development Department of the General Electric Company at Schenectady, N. Y. He joined the RCA Victor Company in Camden, N. J., in 1930, as Manager of Tube Application Engineering. He transferred to Harrison in 1933, and for various periods had charge of power-tube development, cathode-ray-tube development, and gas and phototube development for the Electron Tube Division. He became Manager of the Harrison Engineering activity, which included engineering on semiconductor devices from its start in 1949 until the formation of the Semiconductor and Materials Division in 1955. In 1956 he became Administrator of Advanced Product Development activity of ETD. Mr. James participated in the GE Advanced Engineering program for two years, and has completed a number of other training assignments, including the Institute for Management program at Northwestern University. He received the *RCA Award of Merit* in 1953. He is a Senior Member of IRE, *Fellow* of the Radio Club of America, and member of the American Association for the Advancement of Science, Theta Tau, and Tau Beta Pi.

DEAN W. CHACE received a BS in Basic Engineering from Princeton University in 1951. He joined RCA in the Washington Office of the Patent Department upon graduation and pursued studies in the George Washington University School of Engineering and School of Law. In 1952, he transferred to the Patent Department in Camden, where he was engaged in the solicitation and prosecution of patents relating to transistor circuits, and continued his law studies at Temple University. He received an LLB degree from Temple University in 1955. He is admitted to practice before the United States Patent Office, the U. S. Court of Customs and Patent Appeals, the U. S. District Court for the District of Columbia, and the U. S. Court of Appeals for the District of Columbia Circuit. He transferred to the Patent Department in Princeton in 1957 and in 1959 was appointed to the position of Administrator, Research with responsibility for general Laboratories administrative matters and the administration of the Applied Research Program under the Director of Research, RCA Laboratories. He has been closely associated in a liaison capacity with the New Business Development activity of the Electron Tube Division since December 1960. He was appointed to the position of Senior Technical Administrator, RCA Laboratories, on January 1, 1962.

Laboratories has produced a valuable understanding of each other's plans and problems.

NEW BUSINESS PROJECTS

In at least two cases, recent RCA Laboratories' research innovation has been swiftly translated into major development efforts by ETD.

One of these is a new class of germanium-silicon thermoelectric power-producing materials that are stable and have a long life and high efficiency (Fig. 3). The development of these materials and of thermoelectric modules in ETD already is contract-supported and has excellent prospects of developing into a profitable and large business in a short period of time. ETD has also undertaken a major development program stemming from research on the production of niobium-tin superconductor wire and ribbon, especially attractive for the development of magnets having extremely high field strength (Fig. 4).

Each of these developments is a research result of major significance. However, it is evident that research breakthroughs and good, even spectacular, engineering development *are not bought* by organization charts. They are clearly the result of the labors of dedicated, hard working, competent—often brilliant—technical people. This is as true of the thermoelectric and superconductor developments as it was and will be of other technical developments that are in a very real sense the life blood of RCA. They cannot be achieved, however, without management support and encouragement. The early and sustained role of the New Business Development activity in these projects has been in a direction to ensure *maximum management attention* to the projects. Although it is difficult to speculate on what might have happened without the New Business Development activity, there is general agreement at the RCA Laboratories that transfer of the thermoelectric work from research to product development proceeded in an

While formal liaison has not been established with other RCA product divisions, ETD has been alert to their needs and has looked to them for advice and suggestions. One of the new business projects, the development of a dry-reed switch, is an out-growth of a direct suggestion by R. Guenther, Manager of DEP's Surface Communications Systems Laboratory in New York. Other projects, either in development or being evaluated, have been undertaken in direct support of other divisions or at their suggestion.

ETD SKILLS AND FACILITIES

The wide range of skills which ETD can bring to bear on the development of new products is striking. High-precision, custom-made products and complex machinery are just as familiar to ETD as high-volume, low-cost products. The skills range from the design and manufacture of massive high-vacuum equipment (e.g., the space chamber at RCA's Astro-Electronics Division and the *C*-Stellarator fusion machine for Princeton University) to the precision assembly of microscopic parts and the controlled doping of sensitive materials. These broad capabilities permit the products currently under development to range from huge vacuum vessels to the controlled and uniform deposition of 0.0005 inch of superconductive material on a 0.002-inch-thick ribbon in long lengths.

In the final analysis, it is these skills that will determine the success of the ETD program of diversification. The New Business Development activity's role is exploration, evaluation, and analysis aimed at ensuring that these skills are concentrated on those non-tube new products with the greatest promise of achieving ETD's ambitious goals.

Fig. 5—Dry-reed switches.

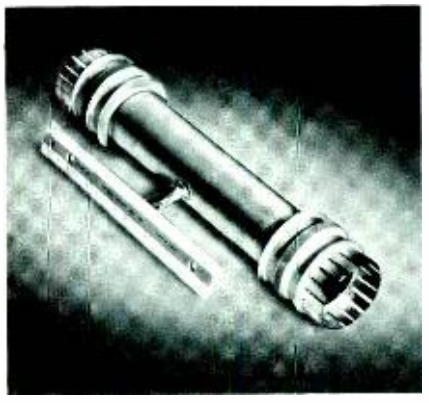
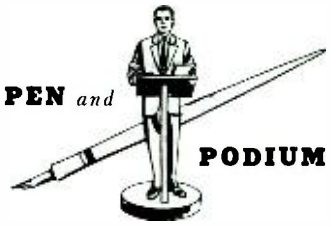


Fig. 6—Thermionic energy converter for power generation. This RCA developmental type Dev. No. A-1190 delivers a power output of 270 watts while heated by radiation.



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The Effects of Ag on Impact Ionization in Cs_3Bi — W. E. Spicer: American Physical Society Meeting, Baltimore, Md., Mar. 24, 1962

Distribution of Electron Bombardment Induced Radiation Defects with Depth in Silicon — H. Flicker, J. J. Loferski: American Physical Society Meeting, Baltimore, Md., Mar. 26, 1962

Theoretical Considerations on Reliability Properties of Recursive Triangular Switching Memories — S. Amarel, J. A. Brzozowski: Symposium on Redundancy Techniques for Computing Systems, ONR, Washington, D.C., Feb. 6, 1962; Proceedings of Symposium

Relations Between Research and Product Divisions in an Industrial Organization — H. W. Leverenz: Professional Group on Military Electronics, Boston Section IRE, Boston, Mass., Mar. 14, 1962

Tunnel-Diode Balanced-Pair Switching Characteristics — J. J. Gibson, G. B. Herzog, H. S. Miller, R. A. Powlus: International Solid-State Circuits Conference, Philadelphia, Pa., Feb. 13, 1962

Semiconducting Materials for Thermoelectric Power Generation — F. D. Rosi: Golden Gate Metals Conference, San Francisco, Calif., Feb. 15, 1962; Proceedings of Conference

Physical Process in Ferroelectric Switching — E. Fatuzzo: Talk at National Bureau of Standards, Washington, D.C., Feb. 28, 1962

Surface Photovoltage Measurements on Cadmium Sulfide — R. Williams: American Physical Society Meeting, Baltimore, Md., Mar. 26, 1962

Radiation Damage in Silicon I: Photovoltaic Response — B. W. Faughnam, and J. A. Baiker: American Physical Society Meeting, Baltimore, Md., Mar. 26, 1962

Radiation Damage in Silicon II: Lifetimes — B. W. Faughnan and J. A. Baiker: American Physical Society Meeting, Baltimore, Md., Mar. 26, 1962

Growth of Codmium Sulfide Crystals with High Impurity Concentration — E. L. Lind and A. B. Dreeben: American Physical Society Meeting, Baltimore, Md., Mar. 26-29, 1962

Properties of Cadmium Sulfide Crystals with High Impurity Concentration—R. H. Bube: American Physical Society Meeting, Baltimore, Md., Mar. 26, 1962

New Ferroelectrics of the Tetramethylammonium Trihao-Mercurate Family — E. Fatuzzo, R. Nitsche: *Physical Review*, Jan. 15, 1962

Measurements of the Dielectric Constant of Rutile (TiO_2) at Microwave Frequencies Between 4.20 and 300°K — E. S. Sabisky and H. J. Gerritsen: *Journal of Applied Physics*, Mar., 1962

DATES *and* DEADLINES

PROFESSIONAL MEETINGS AND CALLS FOR PAPERS

Meetings

May 21-23, 1962: NATL. SYMP. ON AEROSPACE INSTRUMENTATION, ISA; Marriott Twin Bridges Motel, Washington, D.C. *Prog. Info.*: C. Creveling, Goddard Space Flight Ctr., Greenbelt, Md.

May 22-24, 1962: NATL. MICROWAVE THEORY & TECHNIQUES SYMP., IRE-PGMTT; NBS Labs. Boulder, Colo. *Prog. Info.*: R. W. Beatty, NBS, Boulder, Colo.

May 23-25, 1962: NATL. TELEMETERING CONF., IRE-PGSET, AIEE, IAS, ARS, ISA; Sheraton Park Hotel, Wash., D.C. *Prog. Info.*: D. G. Mazur, Code 620, Goddard Space Flt. Ctr., Greenbelt, Md.

May 23-25, 1962: 16TH NATL. ASQC CONV., Netherlands Hilton Hotel, Cincinnati, O. *Prog. Info.*: M. J. O'Callaghan, Schick, Inc., Lancaster, Pa.

May 23-26, 1962: ACOUSTICAL SOC. OF AMERICA, New York City. *Prog. Info.*: W. P. Mason, Bell Telephone Labs, Murray Hill, N. J.

May 24-26, 1962: IRE 7TH REGION CONF. ON SPACE COMMUNICATIONS, Olympic Hotel, Seattle, Wash. *Prog. Info.*: T. G. Dalby, 3220-99th N.E., Bellevue, Wash.

June 10-14, 1962: 1962 ASME SUMMER ANNUAL MTG., Chateau Frontenac, Quebec, Canada.

June 18-19, 1962: SPRING CONF. ON BROADCAST & TV RECEIVERS, IRE-PGBTR, Chicago Sect.; O'Hare Inn, Chicago, Ill. *Prog. Info.*: A. Cotsworth, Zenith Radio Corp., 6001 W. Dickens Ave., Chicago 39, Ill.

June 18-21, 1962: 4TH US NATL. CONGRESS OF APPLIED MECHANICS, U.S. Natl. Comm. on Theoretical & Applied Mechanics (AIChE, AMS, APS, ASCE, ASME, IAS, SESA); Univ. of Calif., Berkeley, Cal. *Prog. Info.*: W. Goldsmith, Dept. of Applied Mechanics, Univ. of Calif., Berkeley 4, Calif.

June 19-21, 1962: AMERICAN PHYSICAL SOC., Evanston, Ill. *Prog. Info.*: K. K. Darrow, American Physical Soc., Columbia Univ., New York 27, N.Y.

June 24-29, 1962: AMERICAN SOC. FOR TESTING MATERIALS ANN. MTG., Statler Hilton and Sheraton-Atlantic Hotels, New York, N.Y. *Prog. Info.*: ASTM Hqrs., 1916 Race St., Phila. 3, Pa.

June 25-27, 1962: 6TH NATL. CONV. ON MILITARY ELECTRONICS (MIL-E-CON), IRE-PGME; Shorcham Hotel, Wash., D.C. *Prog. Info.*: J. J. Slattery, F316, The Martin Co., Baltimore 3, Md.

June 25-30, 1962: SYMP. ON ELECTROMAGNETIC THEORY AND ANTENNAS; The Technical University of Denmark, Oster Voldgarde 10C, Copenhagen K., Denmark. *Prog. Info.*: H. Lottrup Knudsen, above address. (*USSR expected to undertake two sessions.*)

June 27-29, 1962: JOINT AUTOMATIC CONTROL CONF., IRE-PGAC, AIEE, ISA, ASME, AIChE; New York Univ., University Hts., NYC. *Prog. Info.*: Dr. A. J. Hornfeck, Bailey Meter Co., 1050 Ivanhoe Rd., Cleveland 10, O.

June 28-29, 1962: 4TH NATL. SYMP. ON RADIO FREQUENCY INTERFERENCE, IRE-PGRFI; Del Webb, Town House Hotel, San Francisco, Calif. *Prog. Info.*: R. G. Davis, Dept. 58-25, Lockheed Missile & Space Co., P.O. Box 504, Sunnyvale, Calif.

July 2-6, 1962: IONOSPHERE CONF., Inst. of Physics & Physical Soc.; London, England. *Prog. Info.*: J. A. Ratcliffe, Radio Res. Sta., Ditton Park, Slough, Bucks, England.

July 9-13, 1962: 1ST INTL. CONF. ON PARAMAGNETIC RESONANCE, IUPAP; Hebrew Univ., Jerusalem, Israel. *Prog. Info.*: Prof. W. Low, Dept. of Physics, The Hebrew Univ., Jerusalem, Israel.

July 16-18, 1962: LUNAR MISSIONS, ARS; Pick-Carter & Statler Hilton Hotels, Cleveland, O. *Prog. Info.*: B. Chifos, ARS, 500 Fifth Ave., New York 36, N.Y.

Calls for Papers

Aug. 27-31, 1962: 67TH SUMMER MTG. MATHEMATICAL ASSN. OF AMERICA AND AMERICAN MATHEMATICAL SOC., Vancouver, British Columbia. *DEADLINE*: **7/6/62** to AMS Hqrs., 190 Hope St., Providence 6, R.I.

Aug. 27-31, 1962: AMERICAN PHYSICAL SOC., Seattle, Wash. *DEADLINE*: Abstracts, **6/22/62** to H. A. Shugart, U. of Calif., Berkeley 4, Calif.

Sept. 3-7, 1962: NATL. ADV. TECHNOLOGY MANAGEMENT CONF., IRE-PGEM, AIEE, ASCE, AIChE, etal; Opera House, Worlds Fair Grounds, Seattle, Wash. *DEADLINE*: **7/3/62** to Georges Brigham, 805 Logan Bldg., Seattle 1, Wash.

Sept. 28-29, 1962: 12TH ANN. BROADCAST SYMP., IRE-PGB; Willard Hotel, Washington, D. C. *DEADLINE*: **6/20/62** to Dr. William Hughes, E.E. Dept., Okla. State Univ., Stillwater, Okla.

Oct. 1-3, 1962: 8TH NATL. COMMUNICATIONS SYMP., IRE-PGCS, Rome-Utica Sect.; Hotel Utica & Municipal Aud., Utica, N.Y. Exhibits. *DEADLINE*: **6/1/62** to George Baldwin, Paris Rd., R.D. 2, Clinton, N.Y.

Oct. 15-18, 1962: SPACE PHENOMENA & MEASUREMENTS SYMP., IRE-PGNS, AEC, NASA; Detroit, Mich. *DEADLINE*: 100-wd abstracts, **7/1/62**; rough draft of paper, **9/1/62** to M. Ihnat, AVCO Corp., 201 Lowell St., Wilmington, Mass.

Oct. 15-19, 1962: AUDIO ENGINEERING SOC. FALL CONV., Barbizon-Plaza Hotel, New York City, N. Y. *DEADLINE*: titles, summaries, manuscripts and/or suggestions, **6/8/62** to: E. H. Roys, RCA Victor Record Div., 501 N. LaSalle St., Indianapolis, Ind.

Oct. 22-24, 1962: ECCANE (EAST COAST CONF. ON AEROSPACE & NAVIGATIONAL ELEC.), IRE-PGANE: Baltimore Sect.; Emerson Hotel, Baltmore, Md. *DEADLINE*: **6/4/62** to Wm. C. Vergara, Dept. 466-2, Bendix Radio, Towson, Md.

Oct. 25-27, 1962: 1962 ELECTRON DEVICES MTG., IRE-PGED; Sheraton Park Hotel, Washington, D.C. *DEADLINE*: Approx. **8/1/62.**

Oct. 30-31, 1962: SPACEBORNE COMPUTER ENGINEERING CONF., IRE-PGEC; Disneyland Hotel, Anaheim, Calif. *DEADLINE*: 4 cps. 1000-wd. summary, **6/15/62** to Dr. R. A. Kudlich, AC Spark Plug Div., General Motors Corp., 950 N. Sepulveda Blvd., El Segundo, Calif.

Nov. 1-2, 1962: 6TH NATL. CONF. ON PRODUCT ENGR. & PRODUCTION, IRE-PGPEP; Jack Tar Hotel, San Francisco, Calif. *DEADLINE*: **6/11/62** to G. F. Reyling, Varian Associates, 611 Hansen Way, Palo Alto, Calif.

Nov. 4-7, 1962: 15TH ANN. CONF. ON ENGINEERING IN BIOLOGY & MEDICINE, IRE, AIEE, ISA; Conrad Hilton Hotel, Chicago, Ill. *DEADLINE*: 50-wd. abstracts, **6/1/62**; 900-wd. digest manuscript, **8/1/62;** to Prog. Committee, P.O. Box 1475, Evanston, Ill.

Nov. 5-7, 1962: NEREM (NORTHEAST ELECTRONICS RESEARCH & ENGINEERING MTG.), IRE; Commonwealth Armory & Somerset Hotel, Boston, Mass. *DEADLINE*: Either complete papers or 400-500 wd. abstracts, in triplicate, plus 50-wd. summaries, by **6/11/62,** to I. Goldstein, Raytheon Company/Box 555, Hartwell Rd., Bedford, Mass.

Nov. 12-14, 1962: RADIO FALL MTG., IRE-PGBTR, RQC, ED, EIA; King Edward Hotel, Toronto, Ontario, Canada. *DEADLINE*: Approx. **7/15/62,** abstracts. *For info.*: V. M. Graham, EIA Eng. Dept., 11 W. 42 St., New York 36, N. Y.

Nov. 12-15, 1962: 8TH ANN. CONF. ON MAGNETISM & MAGNETIC MATERIALS, IRE-PGMTT, AIEE, AIP; Penn-Sheraton, Pitts., Pa. *DEADLINE*: Approx. **8/18/62.** *For info.*: Prof. Fredk. Keffer, Physics Dept., Univ. of Pitts., Pittsburgh 13, Pa.

Nov. 16-17, 1962: 2ND CANADIAN IRE SYMP. ON COMMUNICATIONS, Queen Elizabeth Hotel, Montreal, Quebec, Canada. *DEADLINE*: In triplicate, 350-wd. summary, subject title, short biographical note. **6/1/62.** Indicate if desire pub. in *Proc.* or *Trans.* To: A. B. Oxley, P. Eng., Canadian IRE Symp. on Communications, Box 802, Station B, Montreal, Quebec, Canada.

Nov. 29-30, 1962: 1962 ULTRASONICS SYMP. IRE-PGUE; New York City. *DEADLINE*: **8/13/62,** to R. N. Thurston, Bell Telephone Labs, Murray Hill, N. J.

Dec. 4-6, 1962: FJCC (FALL JOINT COMPUTER CONF.), AFIPS (PGEC, AIEE, ACM); Sheraton Hotel, Philadelphia, Pa. *DEADLINE*: Abstract, summary and paper, **7/1/62,** to E. G. Clark, Burroughs Research Ctr., Paoli, Pa.

Dec. 6-7, 1962: IRE CONF. ON VEHICULAR COMMUNICATIONS, IRE-PGVC; Mayfair Hotel, Los Angeles, Calif. *DEADLINE*: **8/15/62,** to W. J. Weisz, Motorola, Inc., Comm. Div., 4545 W. Augusta Blvd., Chicago 51, Ill.

Feb. 11-15, 1963: 3RD QUANTUM ELECTRONICS CONF., IRE, SFER, ONR; Paris, France. (Exhibition of working experiments & advanced devices—Feb. 8-15.) *DEADLINE*: Resumé, **11/1/62,** to Madame Cauchy, Secrétaire, 3ème Congrès d'Electronique Quantique, 7, Rue de Madrid, Paris VIIIe, France.

April 17-19, 1963: INT'L SPECIAL TECH. CONF. ON NON-LINEAR MAGNETICS, IRE-PGEC, PGIE, AIEE; Shoreham Hotel, Washington, D.C. *DEADLINE*: **11/5/62,** to J. J. Suozzi, BTL Labs, Whippany, N.J.

May 20-22, 1963: NATL. SYMP. ON MICROWAVE THEORY & TECHNIQUES, IRE-PGMTT; Miramar Hotel, Santa Monica, Calif. *DEADLINE*: **1/19/63,** to Dr. Irving Kaufman.

June 19-21, 1963: JOINT AUTOMATIC CONTROL CONF., IRE-PGAC, AIEE, ISA, ASME, AIChE; Univ. of Texas, Austin, Tex. *DEADLINE*: Abstracts, **9/30/62,** manuscripts, **11/1/62,** to Otis L. Updike, Univ. of Virginia, Charlottesville, Va.

Sept., 1963: 2ND CONGRESS, INTL. FED. OF AUTOMATIC CONTROL CONF., IRE-PGAC, IFAC, AACC; Basle, Switzerland. *DEADLINE*: 200-wd abstract, **6/1/62,** to Dr. Gerald Weiss, EE Dept., Polytechnic Inst., 333 Jay St., Brooklyn 1, N.Y.

Be sure DEADLINES are met — consult your Technical Publications Administrator for lead time needed to obtain required RCA approvals.

Excitons at the L Absorption Edge in Zinc-Blende-Type Semiconductors — M. Cardona and G. Harbeke: *Physical Review Letters*, Feb. 1, 1962

Reflectivity by Gray Tin Single Crystals — M. Cardona and D. L. Greenaway: *Physical Review*, Feb. 15, 1962

The Nature of One-Ion of the Ferrimagnetic Anistrophy — P. J. Wojtowicz: *Journal of Applied Physics*, Mar., 1962

High Temperature Susceptability of Garnets: Exchange Interactions in Yig and LuIG — P. J. Wojtowicz: *Journal of Applied Physics*, Mar., 1962

Symmetry of Transistion Metal Impurity Sites in Crystals as Inferred From Optical Spectra — H. A. Weakliem and D. S. McClure: *Journal of Applied Physics*, Jan., 1962

Basic Switching Devices and Circuits — B. J. Lechner: AIEE-N.Y. Section, Winter Study Group, Jan. 22, 1962

ELECTRON TUBE DIVISION

Program Evaluation Review Techniques — E. J. Homer: Northern New Jersey Section Meeting, American Society of Mechanical Engineers, Newark, N. J., Jan. 16, 1962

Plans for the RCA-301 at RCA Electron Tube Division — W. K. Halstead: RCA-501 Users Meeting, Washington, D. C., Feb. 13, 1962

Nuvistor Two-Meter Transmitter — R. M. Mendelson: *RCA Ham Tips*, Feb., 62

Circuits to Control and Protect High-Power Modulator Tubes — T. E. Yingst: *Electronics*, Jan. 12, 1962

RCA Research on Phosphors for CR Tube Use — A. L. Smith: Graduate Seminar at the University of Connecticut, Jan. 17, 1962

The Accounting Responsibility to Research — W. G. Fahnestock: Lancaster Chapter Meeting, National Association of Accountants, Lancaster, Pa., Jan. 19, 1962

The Coaxitron, A High-Power, Broadband, Integral-Cavity UHF Amplifier — F. S. Keith, W. N. Parker and C. L. Rintz: AIEE Winter General Meeting, New York City, Jan. 28-Feb. 2, 1962

Low-Duty-Cycle Tunnel-Diode Tester — L. M. Zappulla: *Electronics*, Jan. 26, 1962

Nuclear Radiation Detectors — G. A. Morton: IRE Section Meeting, Lancaster, Pa., Feb. 27, 1962

A System Designer Surveys the Radio Spectrum — D. J. Blattner: IRE Westchester Subsection Lecture Series, Feb. 28, 1962

Microwave-Carrier Modulation-Demodulation Amplifiers and Logic Circuits — F. Sterzer and W. Eckhardt: *Proceedings of IRE*, Feb., 1962

SEMICONDUCTOR AND MATERIALS DIVISION

Application of Silicon Rectifiers — R. H. Pollack: USAF Eastern Technical Radio Net, Feb. 4, 1962

New Materials for Primary and Secondary Batteries — G. S. Lozier: *IRE Transactions on Military Electronics*, Jan., 1962

Characteristics of GaAs Solar Cells with Greater Than 12% Conversion Efficiency — M. F. Lamorte, A. Gobat and G. McIver: *IRE Transactions on Military Electronics*, Jan., 1962

Functional Approach to Critical Measurements of Organic Dielectrics — J. M. Schiller: *Electro-Technology*, Jan., 1962

Transistor Applications — F. B. Smith: USAF Eastern Technical Radio Net, Jan. 21, 1962

Unipolar Transistors — J. A. Olmstead: IRE Section Lecture Series, Cleveland, Ohio. Jan. 25, 1962

General Discussion of Semiconductor Devices — E. O. Johnson: USAF Eastern Technical Radio Net, Jan. 28, 1962

Statistical Optimization of a Transistor Production Line — P. J. Veringa and G. Garfinkel: Rutgers University Seminar, New Brunswick, N. J., Feb. 7, 1962

Zero-Bias Sweep-Tube Modulators — G. D. Hanchett: *QST*, Feb., 1962

Heat Treatment of N-Type GaAs by Radiant Energy — T. Kinsel and T. Seidel: *Journal of Applied Physics (Letters)*, Feb., 1962

Absorption Edge in Degenerate P-Type GaAs — I. Kudman and T. Seidel: *Journal of Applied Physics*, Feb., 1962

An All-Transistor Six-Meter Receiver — S. W. Daskam and A. Troiano: *QST*, Feb., 1962

The Effects of Transistor Parameters on Surge-Voltage Transients in Rectifier Circuits — P. E. Kolk: *Electronic Equipment Engineering*, Feb., 1962

BROADCAST AND COMMUNICATIONS PRODUCTS DIVISION

Alignment of Microwave Antennas — J. B. Bullock: *Broadcast News*, Dec., 1961

New 20 KW FM Transmitter — I. H. Lubash: *Broadcast News*, Dec., 1961

The Design of a New Solid State Tone Multiplex Equipment — F. M. Brock: Pennsylvania Electric Association, 1962 Winter Meeting, Philadelphia, Pa., Jan. 26, 1962

Slant Track Video Recorders — A. H. Lind: SMPTE, New York Section, Feb. 14, 1962

Small Boat Electronics — Present and Future — N. L. Barlow: U. S. Power Squadron National Convention, Miami Beach, Florida. Jan. 12, 1962

Stabilization of Monochrome and Color-TV Cameras—K. Sadashige and H. N. Kozanowski, Goth SMPTE Conv., Lake Placid, N.Y., Oct. 1-6, 1961.

RCA VICTOR RECORD DIVISION

Average Vs. R.M.S. Meters for Measuring Noise — J. J. Davidson: *IRE Transactions on Audio*, July-Aug., 1961.

The Education of an Electroplater — A. M. Max: American Electroplaters Society. Indianapolis, Ind., Jan. 12, 1962

The Application of Electroforming to the Manufacture of Disc Records — A. M. Max: ASTM Symposium on Electroforming, Dallas, Tex., Feb. 6, 1962

The Disc Phonograph Record — A. M. Max: Indianapolis Sigma Xi and R.E.S.A., Feb. 21, 1962

ELECTRONIC DATA PROCESSING

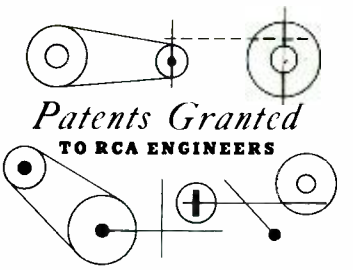
Modern Developments in Data Communication — J. Wesley Leas: Association of Research Directors in New York City, Jan. 18, 1962

Gigacycle Computer Techniques — J. N. Marshall: AIEE Winter General Meeting, Jan. 30, 1962

The Design and Performance of a Magnetic Tape Data Transmission Terminal — C. N. Batsel, Jr., R. E. Montijo, Jr., J. P. Reid and W. Saeger: AIEE Winter General Meeting, Jan. 31, 1962

Data Communication Coordination in an RCA Magnetic Tape Terminal — R. E. Montijo, Jr., W. Saeger, R. J. Sibthorp and E. F. Wesley: AIEE Winter General Meeting, Jan. 31, 1962

Design of a Single Channel ARQ System — J. J. O'Donnell and C. D. Hughes: AIEE Winter General Meeting, Jan. 31, 1962



AS REPORTED BY RCA DOMESTIC PATENTS, PRINCETON

DEFENSE ELECTRONIC PRODUCTS

3,015,075—Signal-Amplitude Responsive Class-B Biasing Circuit, Dec. 26, 1961; P. L. Bargellini

3,020,450—Mounting for Electrical Elements, Feb. 6, 1962; R. E. Shafer

3,018,389—Delay Circuit Using Magnetic Cores and Transistor Storage Devices, Jan. 23, 1962; M. B. Herscher

3,018,391—Semiconductor Signal Converter Apparatus, Jan. 23, 1962; J. E. Lindsay and T. B. Martin

3,023,963—Digital Computing Systems, Mar. 6, 1962; E. J. Schmitt and J. Smith

3,023,964—Digital Computing Systems, Mar. 6, 1962; L. S. Bensky and I. H. Sublette

3,024,445—Information Transferring System, Mar. 6, 1962; A. M. Spielberg and J. F. Page

3,025,411—Drive Circuit for a Computer Memory, Mar. 13, 1962; W. G. Rumble

3,026,413—Determining the Range of an Infrared Source with Respect to a Point, Mar. 20, 1962; P. K. Taylor

3,026,420—Magnetic Switching and Storing Device, Mar. 20, 1962; R. L. Whitely

3,026,504—Information Transmission System, Mar. 20, 1962; J. A. Aurand and L. S. Lappin

HOME INSTRUMENTS DIVISION

3,023,271—Chroma Converter, Feb. 27, 1962; R. B. Hansen

3,020,357—Resonant Circuitry for a Transducer Head, Feb. 6, 1962; M. J. Nowlan

3,026,373—Dual Feedback Circuit for Stereophonic Audio-Frequency Signal Amplifier Systems, Mar. 20, 1962; R. S. Fine and S. V. Perry

3,026,378 — Stereophonic Audio-Frequency Amplifier System, Mar. 20, 1962; R. S. Fine and S. V. Perry

3,027,109—Magnetic Recording and Reproducing Equipment, Mar. 27, 1962; D. R. Andrews, E. S. Maris

3,027,110—Recording and Reproducing Apparatus, Mar. 27, 1962; D. R. Andrews

3,027,111—Recording and Reproducing Apparatus, Mar. 27, 1962; G. E. Redfield, E. S. Nesenger

ELECTRONIC DATA PROCESSING

3,018,042—Data Input System, Jan. 23, 1962; D. L. Nettleton

ELECTRON TUBE DIVISION

3,020,619—Firing Process for Forsterite Ceramics, Feb. 13, 1962; W. J. Koch

3,020,444—Travelling Wave Tube Coupler, Feb. 6, 1962; H. J. Wolkstein & R. E. Bridge

3,023,555—Automatic Traying Apparatus, Mar. 6, 1962; C. G. Schesch

3,024,300—Vacuum Seal for Electron Tubes, Mar. 6, 1962; I. E. Martin

3,025,944—Article Orienting and Positioning Device, Mar. 20, 1962; K. R. Sloan & H. W. Baer

3,026,438—Grid-Cathode Assembly for Cathode Ray Tubes, Mar. 20, 1962; T. P. Warne, Jr.

3,027,479—Electron Guns, Mar. 27, 1962; R. E. Benway

3,027,482—Lime Glass Article Having a Surface or Reduced Resistivity, Mar. 27, 1962; J. L. Gallup

PRODUCT ENGINEERING

3,026,411—Clock Controlled Receiver, Mar. 20, 1962; G. L. Beers

Organization of a Gigacycle Computer — P. Warburton: AIEE Winter General Meeting, Feb. 1, 1962

Some Considerations in Kilomegacycle Computer Design — D. R. Crosby: AIFE Winter General Meeting, Feb. 4, 1962

Digital Communications for Data Processing — J. L. Owings: IRE, Philadelphia, Pa., Feb. 19, 1962

DEFENSE ELECTRONIC PRODUCTS

Neuron and Neural Logic — F. Putzrath: Northwestern University, Jan. 11. 1962

RCA Multifont Reading Machine — W. J. Hannan: Symposium on Character Recognition, Washington, D. C., Jan. 15, 1962

Solid-State Interconnection Problems — A. H. Coleman: 1962 International Solid State Circuits Conference, Philadelphia, Pa., Feb. 14. 1962

The Semiconductor Delay Line and Related Devices — J. J. Seine and S. N. Levine: 1962 International Solid State Circuits Conference, Philadelphia, Pa., Feb. 15, 1962

Broadband Parametric Amplifiers by Simple Experimental Techniques — B. Bossard: AIEE 3rd Winter Convention on Military Electronics, New York City, Feb. 2. 1962

Bandwidth of Hybrid-Coupled Tunnel Diode Amplifiers — R. M. Kurzrok: *IRE Proceedings*, Correspondence, Feb., 1962

Jamming Vulnerability of Communications Systems — A. B. Glenn: *IRE Transactions on Communications Systems*, Sept., 1961

Organizing A Design Review Program — L. Jacobs: American Management Association Meeting, Chicago, Ill., Mar. 2. 1962

Series Regulator Nomograph — R. I. Wolfson: *Electronic Design*, Feb. 15. 1962

Automatic Checkout for Aerospace Vehicles — R. J. Allen: UCLA Lecture on Automatic Checkout for Aerospace Vehicles, Oct., 1961

Sensing Systems for North American Defense — C. L. Conner: U. S. Naval Research Reserve Company, Oak Ridge, Tenn., Jan. 10, 1962

Bionics — T. B. Martin: AIEE-IRE Student Group, University of Pennsylvania, Jan. 22, 1962

Fiber Optics — A New Tool in Electronics — L. J. Krolak: Canadian Section of SMPTE. Montreal, Quebec, Canada, Mar. 7. 1962

Satellite Rendezvous — P. Nesbeda, Brown Univ., Mar. 7 1962.

Data Processing — E. T. Hatcher, Moorestown Rotary Club, Oct. 26, 1961.

Engineering  **NEWS** *and* **HIGHLIGHTS**

SC&M PRESENTS ENGINEERING ACHIEVEMENT AWARDS

The Semiconductor and Materials Division honored its engineers at the Division's third annual *Engineering Achievement Award* presentation in Somerville on February 21. **Dr. Alan M. Glover,** Vice-President and General Manager of the Division, presented the awards.

The following engineering teams received special recognition:

Leonard P. Fox, Ernest W. Karlin, Richard C. Pinto, and **Steven G. Policastro,** "*. . . for combined accomplishments in the engineering of the* MINUTEMAN *transistor program.*"

Lewis Jacobus, Robert E. Kleppinger, Raymond A. Santilli, C. Frank Wheatley, and **John D. Young,** "*. . . for combined accomplishments in the design, application, and manufacture of a complement of RCA devices for the fully transistorized auto-radio circuit.*"

Edgar D. Casterline, Henry J. Krautter, Robert M. Minton, and **Leroy W. Varrettoni,** "*. . . for combined accomplishments in the engineering of the tunnel diode for special projects.*"

A joint award was made to **Eugene C. Fortine** and **Howard Lessoff,** of Needham, Massachusetts, "*. . . for outstanding performance in the development of high-temperature ferrite memory cores.*"

In recognition of outstanding performance, individual awards were presented to:

William A. Bentley, "*. . . for superior knowledge of our products and technology, combined with commercial instinct, leading to full application of our products to auto-radio circuitry.*"

Gerald S. Lozier, "*. . . for technical leadership in the field of electro-chemistry and for specific contributions in the areas of high-capacity battery development.*"

Peter A. Peckover, "*. . . for demonstrating exceptional initiative and creative ability in the development of techniques and equipment for testing semiconductor products.*"

John D. Young, "*. . . for superior technical understanding applied imaginatively to the reduction of manufacturing costs and increases in yields in drift field transistors.*"

DR. ENGSTROM NAMED FOR EIA MEDAL OF HONOR

Dr. Elmer W. Engstrom, President of RCA, has been named by the Electronic Industries Association Board of Directors to receive the association's highest award, the *EIA Medal of Honor.* The medal has been given annually since 1952 for "*distinguished service contributing to the advancement of the electronics industry.*" It will be presented Dr. Engstrom May 24, at the yearly EIA award dinner, held in conjunction with the association's annual convention in Chicago.

Dr. Engstrom was the second RCA executive to be selected for the metal. It was first given in 1952 to **Brig. General David Sarnoff,** Chairman of the RCA Board, who at a recent EIA Government-Industry Dinner was presented a scroll of a special EIA Board resolution memorizing his devotion of 55 years to electronics progress.

RCA SALES AND EARNINGS SET ALL-TIME FIRST QUARTER RECORD

January-March 1962 marked *the highest first-quarter sales and earnings in the 43-year history of RCA.* Profits after taxes rose 21 percent to $14,500,000, compared with $12,000,000 for the first quarter of 1961. The previous record for first-quarter earnings was $13,000,000 in 1960. Earnings per common share for the first quarter of this year were 81 cents, compared with 68 cents in the same period of 1961 on a slightly smaller volume of shares outstanding.

Sales of products and services increased 81 percent to $425,000,000, compared with the previous record of $361,700,000 for the same 1961 period. The profit and sales records reflected a major upsurge in all principal areas of RCA's business. Color television receivers and color picture tubes continued to set the pace in consumer products and components. Carrying forward the trend established in the fourth quarter of 1961, dollar earnings from the sale of color TV sets again exceeded those of black-and-white set sales. At the same time, black-and-write receiver sales maintained a steady improvement.

Progress in electronic data processing contributed to improved profits through reduction in costs and increased sales volume. Defense and space activities maintained their strong cycle of growth. RCA now has contracts involving seven major satellite projects. The National Broadcasting Company set an all-time first-quarter record in both sales and earnings.

COLOR TV TUBES TO BE MADE AT INDIANA PLANT TO MEET RISE IN DEMAND

Plans are underway for the second major addition this year to RCA color-television picture-tube production facilities, to meet industry demand. A $1.7 million program has been approved to inaugurate color tube production at the RCA plant in Marion, Indiana. Recently, plans were announced for a $1.5 million expansion of the Lancaster, Pa., color picture tube manufacturing plant. Two color-tube production lines are planned for operation at Marion before the end of this year. This plant also will continue to make more than 100 different types of black-and-white picture tubes.

NBC ADDS FILM STUDIO AND EXPANDS VIDEO TAPE FACILITIES

A new film studio for network operations was completed at the NBC Film Exchange Building in Englewood, New Jersey in March. The studio is equipped with two RCA TK-26 color cameras. Half-hour and one-hour color shows will originate from this location.

Two new RCA TRT-1B video tape recorders are being installed in New York to be ready for daylight saving time. These recorders will be equipped with line-lock and pix-lock. This will make a total of 22 video tape recorders used by NBC in New York.—*W. A. Howard*

RCA ADVANCES IN MICROWAVE COMPONENTS AND SOLID CERAMIC CIRCUITS HIGHLIGHTED AT IRE SHOW

A major advance in microwave semiconductor devices and the first public showing of solid ceramic microelectronic circuits highlighted the Semiconductor and Materials Division exhibit of many new devices at the annual convention of the IRE at the New York Coliseum, March 26-29, 1962.

The microwave devices advance is RCA's new gallium arsenide varactor diode which has the highest operating frequency of any GaAs junction device on the market. *(See Gibbons, et. al., this issue.)*

The new solid ceramic circuits represent an important advance in microelectronic technology. One-third the size of an aspirin tablet, this developmental device can perform all conventional circuit functions from amplification to computer switching and lends itself to mass production by assembly line printing techniques. *(See Kihn, this issue.)*

NEW BUILDINGS AT AED-PRINCETON WILL INCREASE ENGINEERING FACILITIES BY 50 PERCENT

More than 100,000 square feet of engineering and administrative space will be added to the *RCA Space Center* (DEP Astro-Electronics Division) near Princeton, N. J., through two new buildings. Further evidence of AED growth lies in the planned delivery of an average of two satellites or space vehicles per month during 1962. The deliveries will include more of the TIROS meteorological-satellite series and satellites for the Project RELAY transoceanic communications experiments. Both are being developed for NASA.

Since 1958, facility additions have increased total engineering space from an original 40,000 to more than 200,000 square feet. These new buildings, which will be completed in the Fall 1962 year, will bring total area to more than 300,000 square feet. The new facilities will consist of two main buildings, each two stories in height. When completed, they will become the front of the Space Center. Because of the increasing role of RCA in the space program, the number of employees at the Space Center is now approaching 1500.

RCA LABORATORIES AID PROSPECTIVE SCIENCE TEACHERS

In cooperation with Trenton State College, RCA Laboratories, Princeton, has established an experimental *Honors Quarter Program* for prospective high-school science teachers. To initiate the program, a Trenton State senior recently spent 10 weeks working full-time as a research technician in the Materials Research Laboratory. The Trenton State senior received credits for his work at the Laboratories and returned to his class work at the end of the 10 weeks. The program is designed to enable the prospective teacher to observe, and work and talk with research scientists so that as a teacher he will be better able to discuss the methods, problems, and opportunities of scientists with his students.

PROFESSIONAL ACTIVITIES

RCA Victor Record Division, Indianapolis: For the Audio Engineering Society Convention, October 15-19, 1962 at the Barbizon Plaza Hotel in New York City, **H. E. Roys,** Chief Engineer, RCA Victor Record Division, will serve as convention chairman. He is also Executive Vice President of the AES. The following engineers are attending the *Transistor Engineering* course being given in the RCA Home Instrument Division, Indianapolis: **A. G. Evans, J. J. Davidson, E. P. Koeppe,** and **H. D. Ward.** Also, **J. J. Davidson** is instructor for one session. At the Audio Engineering Society Convention in October, 1961, **Arthur G. Evans** was elected *Fellow.—M. L. Whitehurst*

Broadcast and Communications Products Div., Camden: **A. H. Lind** will be a Session Chairman (Broadcast Audio) at the upcoming Audio Engineering Society Convention, Oct. 15-19, 1962 in New York. **J. E. Volkmann** will be a Session Chairman on Sound Reinforcement and Acoustics.
—M. L. Whitehurst

EDP, Cherry Hill, N. J.: **J. Wesley Leas,** Chief Engineer, EDP, has been appointed General Chairman of the Fall Joint Computer Conference which will be held at the Sheraton and Bellevue-Stratford Hotels in Philadelphia, December 4-6, 1962. Other RCA members of Mr. Leas' committee include **R. A. C. Lane,** Exhibits, and **T. T. Patterson,** Administration.—*T. T. Patterson*

DEP Central Engineering, Camden: **V. R. Monshaw,** of Activity 411, is Treasurer and Chairman of Finance Committee for the Ninth National Symposium on Reliability and Quality Control which will be held in San Francisco on January 22-24, 1963. **Paul L. Neyhart,** of Activity 416, is a member of the Program Committee for the Philadelphia Section of IRE Professional Group on Reliability and Quality Control.
—P. F. Kennedy

DEP-SurfCom, Camden: **O. B. Cunningham,** Chief Engineer, Surface Communications Division, was Chairman of Technical Session 35, *New Views of Industrial Electronics,* at the IRE International Convention in New York on March 28, 1962.
—C. W. Fields

DEP Applied Research, Camden: In February, 1962, **E. J. Denlinger** became a member of the Phi Kappa Phi Scholastic Honorary Society at the Pennsylvania State University.—*M. G. Pietz*

Home Instruments Div., Indianapolis: A course in *Management Economics* was conducted by **H. McGuff** of Indiana Central College and was completed in January. All leaders and managers in H. I. engineering attended this school. A series of 14 lectures in *Transistor Circuitry* is being conducted now for H. I. engineering.

DEP-MSR, Moorestown: **W. W. Pleasants,** Manager of Construction and Emplacement, BMEWS presented a talk on the BMEWS System on April 2, 1962 for the high school students who were elected officials of Deptford Township during their *Youth Week.—T. T. Greene*

Product Engineering, Camden: **C. M. Sinnett** spoke to Drexel Institute of Technology graduate engineering students on *Creativity* on March 8, 1962.

RCA 301 BEING IMPLEMENTED AT DEP-DSD, VAN NUYS FOR ENGINEERING AND ADMINISTRATIVE USES

An RCA 301 computer system has been installed at the DEP-Data Systems Div., Van Nuys, Calif., consisting of a processor, card reader, printer, tape stations, and card punch. As this initial system becomes heavily utilized, additional RCA 301 equipment will be considered, which may include simultaneous mode control, additional tape stations, higher speed tape stations, random access disk files, and an additional printer or card reader.

The initial programs being implemented will replace the present punch card calculator, at a saving of around $1000 per month in rental. The next planned step is to convert accounting and payroll operations from punch-card to computer handling—as permanent parts of the ultimate integrated computer system. Approximately 50% of the systems work and programming is completed.

The ultimate system will include, but will not be limited to, the following: engineering-drawing and bill-of-material information will be transferred to magnetic tape. Product requirements will be matched in analysis runs with these magnetic tape files and requirements for labor, facilities, and material produced. Plant schedules will be prepared. Material requisitions will be matched with magnetic tape inventory files. Releases from inventory and purchase requisitions will result. Purchase requisitions will be matched with vendor files on magnetic tape and purchase orders printed as well as a purchase order suspense file maintained on magnetic tape. Material receipts and invoices will further update the purchase order suspense file and at the appropriate time check registers and vendor checks prepared.

It is expected that one of the largest uses of the RCA 301 will be for engineering calculations and analysis. Special equipment and techniques will be used for this work as the need develops. PERT will be one of the first engineering applications.
—D. J. Oda

DR. SHAW, FORMER ETD CHIEF ENGINEER, HONORED FOR HIS 41-YEAR DISTINGUISHED CAREER

On January 9, 1962, more than 200 associates of **Dr. G. R. Shaw** gathered at the Essex House Hotel, Newark, New Jersey, to pay him tribute on the occasion of his retirement from the RCA Electron Tube Division. After 41 years of association, both RCA and the industry at large lost one of its most dedicated scientific workers, executives, and finest gentleman. With Dr. Shaw and Mrs. Shaw at the head table were **Dr. G. H. Brown, D. F. Schmit, E. M. Tufts, D. Y. Smith, L. W. Teegarden, W. M. James,** and **J. T. Cimorelli.** Many other distinguished gentlemen representing RCA and the industry from other sections of the country were also in attendance. Fond memories were recalled as the master of ceremonies, J. T. Cimorelli, gave a biographical sketch of the interesting highlights of Dr. Shaw's distinguished career.

All members of the Electron Tube Division and the entire Corporation hold Dr. Shaw in deep respect and are proud to have been associated with him. Best wishes go out to him for continued health and happiness.
—T. M. Cunningham

BITTING NAMED SLOAN FELLOW

R. C. Bitting, MINUTEMAN Program Manager, Communications and Aerospace, DEP, Camden, has been awarded an *Alfred P. Sloan Fellowship in Executive Development* at the M.I.T. School of Industrial Management. He is one of 41 young business executives selected. The Sloan Fellows will move with their families to the Cambridge, Mass., area in June to begin a year of intensive study. Many of the 41 *Fellows* will complete M.I.T.'s requirements for an MS in Industrial Management.

Mr. Bitting, who is 37, started with RCA in 1949 after receiving a BS in Physics from Bucknell University. He has since completed his course credits for an MSEE at the University of Pennsylvania. Before being named MINUTEMAN Manager, Mr. Bitting was Manager, Engineering Projects in the Surface Communications Division, DEP, Camden.

In addition to the awards granted by the Sloan Foundation to help defray costs, Mr. Bitting will continue to receive his salary from RCA, which will also pay other expenses associated with the program.

DSD STARTS AFTER-HOURS COURSE ON DIGITAL TECHNIQUES

The DEP Data Systems Division, Van Nuys, Calif., has started the first of a series of full scale, after-hours Engineering courses. The first course will be covered in 36 weekly sessions and is taught by several DSD engineers. Content consists primarily of practical logic and circuit-design techniques employed by the engineers of the Digital Systems Design and Development Group, and descriptions of equipments designed by the group.—*D. J. Oda.*

EDP TRAINING PROGRAM ASSUMES INTERNATIONAL ASPECT

The Training activity of EDP Service Division, RCA Service Company, Cherry Hill, N. J., directed by **M. H. MacDougall,** has for several years trained engineers and technicians in the operation and maintenance of RCA 301 and 501 equipment. Revently, with the sale of RCA 301 systems to ICT in England, Machines Bull in France, and HiTachi in Japan, and the installation of RCA 301 and 501 systems in Sweden, training programs have been conducted for English, Swedish, and French personnel in Cherry Hill. A maintenance training program is also being conducted by an EDPS instructor in Paris for Machines Bull personnel. Upon return to their home countries, they will be involved in the installation and maintenance of RCA 301 systems, and in the training of additional engineers and specialists.—*J. Lawler.*

EXPERIMENTAL COLOR CAMERA PRODUCES TV PICTURES IN RICH HUES AND FINE DETAIL

An experimental, four-tube color-TV camera. the TK-42X, which produces color pictures in richer hues and finer detail than ever before attained, was demonstrated for the first time at the recent NAB Convention in Chicago. Its most striking innovation is the addition of a fourth pickup tube to provide a separate monochrome or *M-channel.* Use of the new camera will not necessitate any change in present color television receivers. As in four-color printing, the imposition of black on the three primary colors enriches the hues and provides sharper definition in the finished picture. The new concept results in a superior black-and-white picture on noncolor receivers.

George DeLong

Bernie Singer

Jim Carter

Merle Pietz

NEW ED REPS NAMED: DeLONG FOR ETD LANCASTER, SINGER FOR EDP PENNSAUKEN, CARTER FOR DEP-DSD BETHESDA, PIETZ FOR DEP APPLIED RESEARCH, CAMDEN.

George A. DeLong has been named to serve as RCA ENGINEER Editorial Representative for Conversion Tube Operations, ETD, Lancaster, Pa., replacing **Wayne Fahnestock.**

In Electronic Data Processing, **Bernie Singer** will represent Data Communications Engineering in Pennsauken, N. J.

For the new Data Systems Center in Bethesda, Md., of the DEP Data Systems Division (headquarters in Van Nuys), **H. James Carter** has been named Editorial Representative, and will serve on **Frank Whitmore's** DEP Editorial Board.

Also in DEP (and on Whitmore's Editorial Board), **M. G. Pietz** has been named as Editorial Representative for DEP Applied Research in Camden, replacing **Wes Whittier.**

The RCA ENGINEER Editors welcome these men, and encourage engineers in their areas to make contact with them on all RCA ENGINEER matters. Their professional backgrounds are as follows:

George A. DeLong served as a Quartermaster in the U. S. Navy from 1940 to 1946. In 1951 he received the AB degree in Liberal Arts from Lebanon Valley College. From 1951 to 1953 he was employed as a salesman by the B. F. Goodrich Company. In April of 1953, he joined the Electron Tube Division of RCA at Lancaster, Pennsylvania where he has served as a Foreman and in 1958 was assigned as an Industrial Engineer in the Conversion Tube Manufacturing and Engineering sections and in the Power Tube Engineering section. Mr. DeLong in 1962 was named as a Project Representative in the Conversion Tube Operations Planning and Control Group at Lancaster.

Bernie Singer joined RCA in 1953 following his discharge from the U. S. Army, where he was an instructor in radar maintenance. From 1953 to 1956 he was engaged in factory systems testing and in 1956 joined EDP as a Technical Writer and Editor, responsible for instruction books and specifications for special data processing equipments. He participated in the BIZMAC II manuals, specifications for the RCA 501 System, proposals for new equipments and systems, progress reports, and documentation of RCA's portion of COMLOGNET. He was named Leader, Engineering Publications in February 1962.

H. James Carter received his BSEE from Tri-State College in 1940. After working for American Airlines, Inc., he joined the Air-Track Manufacturing Corp. in College Park, Maryland and was assigned the design problems associated with radar training devices. He later acted in liaison between the editorial department and the project engineers, subsequently becoming Editor. From 1947 to 1957 he was Director of Publications for the Maryland Electronic Manufacturing Corp. in College Park, and when this company was bought by Litton Industries, he continued to supervise the group. In 1959 Mr. Carter joined Entron, Inc., Bladensburg, Maryland, where he was responsible for systems manuals, employee's *Newsletter*, the advertising program; and public, employee, and customer relations; he was also acting Sales Manager. In February 1962, Mr. Carter joined RCA at the new Bethesda Data Systems Center where he is assigned to project ACSI-MATIC. He is a Senior Member of the IRE and an active member of PGEWS and PGEM, and of the Society of Technical Writers and Publishers.

M. G. Pietz graduated from the University of Florida in 1960 with a BS in physics. He joined RCA's specialized training program for engineers and scientists after graduation. During the training program he worked on microminiature circuits, advanced techniques for optical tracking, magnetic domain theory and optical correlation techniques utilizing Electrofax. His last assignment on the training program was with DEP Applied Research, and he is now assigned to the publications group of Applied Research. He attended the Technical Writer's Institute at Rensselaer Polytechnic in 1961, and is active in the STWP.

A. N. PINSKY NAMED TO HANDLE TREND

A. N. Pinsky has been named Administrator, Professional Development Communications, to assist **C. M. Sinnett,** Director, Product Engineering Professional Development, in the publication of TREND, RCA's research and engineering news digest.

Mr. Pinsky formerly worked in DEP-ACC's Reports and Proposals group in Camden. Before that he was a senior technical writer at the Burroughs Corporation Research Center in Paoli, Pa. He received a BS in 1943 from the University of Connecticut. As a Marine Lieutenant during World War II, he completed special courses in electronics at the Harvard University Graduate School of Engineering and M.I.T. After the war he became a newspaperman and was city editor of the *Elkhart Truth* in Elkhart, Ind., and the *Evening Press* in Levittown, Pa.

TREND is published to improve communications between management and engineering personnel and to provide RCA scientists and engineers with a better understanding and appreciation of the Corporation's activities. Its news items cover professional activities, scientific advances, policy, new markets, awards, and business. Suggestions to make TREND more useful to its readers are welcomed by the TREND Editorial Board and may be addressed to *A. N. Pinsky, 2-8, RCA, Camden, N. J.*

Al Pinsky (left) and C. M. Sinnett

NEW REFERENCE PUBLICATION ON RF INTERFERENCE

The IRE Professional Group on RF Interference has devoted a new issue of its *Transactions* (RF-4, No. 1) to the presentation of a bibliography on RFI literature. Intended as a working reference, the bibliography was prepared by the Engineering Experiment Station at Georgia Institute of Technology, and by **R. F. Flikki,** DEP-SurfCom, Camden. If not available in RCA Libraries, those interested in obtaining this special issue should contact the IRE Office, 1 East 79 St., New York City 21, N. Y.

—C. W. Fields

QSL CARDS OFFERED TO RCA HAMS

RCA employees who are amateur radio operators may obtain distinctive new QSL cards that features the corporate emblem, and their call letters. Name, address, and call letters are on the front of the card; the reverse side is reserved for technical information, comments, and recipient's address. Any licensed radio amateur in RCA may obtain these QSL's in lots of 300 cards at the special price of $5.00. Orders should be sent to the *Cashier, Building 19-2, RCA Electron Tube Division, Harrison, New Jersey,* and should be accompanied by a check for $5.00 payable to *Radio Corporation of America,* together with imprint information (call letters, name and address) as it is to appear on the cards. The cards will be forwarded by intracompany mail.

—J. F. Hirlinger

DEP-MSD ESTABLISHES TECHNICAL PUBLICATION AND PRESENTATION COMMITTEE

To encourage and coordinate the best in engineering presentations and published papers, the DEP Major Systems Division, Moorestown, has established a unique MSD Technical Publication and Presentation Committee. Some key objectives of the MSD Committee are to:

1) review requests for material and announcements of scheduled meetings and promote appropriate attendance by MSD personnel;
2) provide recommendations to MSD management on participation in society committees;
3) recommend subjects on which MSD personnel should prepare papers, and review abstracts of prospective papers to help promote greater acceptance of MSD-prepared material;
4) help assure that submission deadlines are met;
5) provide guidance and assistance in securing necessary RCA and government clearances for release of the information concerned.

Members of this committee are: **I. N. Brown,** Chairman and Systems Engineering Representative; **W. L. Campbell,** Marketing Representative; **H. Eigner,** Project Engineering Representative; **K. I. Pressman,** Program Control and Subcontracting Representative; **R. R. Welsh,** Advanced Systems Planning Representative; and **L. L. Evans,** Field Operations Representative. Mr. Brown is also RCA ENGINEER Editorial Representative for MSD, and assists **F. D. Whitmore,** DEP Technical Publications Administrator on matters of engineering-paper approval affecting MSD.

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